



SL6550

Near Field Communication (NFC) Controller

Product Data Sheet

NFC makes life better!



Rev.1.0

17.Jun.2020

Beijing Smartlink Microchip Co.Ltd.®

Revision History

Version	Release Data	Prepared By	Description
V0.1	27.Mar.2020	Smartlink Microchip	Initial release.
V0.2	1.Apr.2020	Smartlink Microchip	Add Functional Description
V1.0	17.Jun.2020	Smartlink Microchip	Add details of power supply and contactless unit interface.

仅供野火参考使用

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1. Introduction

This document mainly introduces the product information of SL6550, an Near Field Communication (NFC) Controller chip. After reading this document carefully, users can have an in-depth understanding of the SL6550 chip's port information and know how to use it. For more detailed information, please connect <http://www.smartlinkmicro.com>.

2. General description

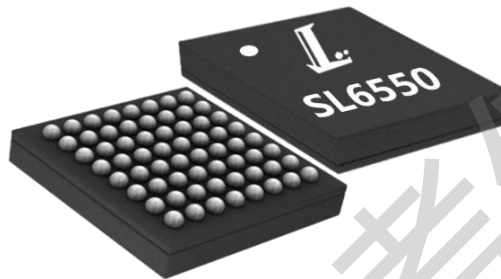


Figure 1. SL6550 NFC Controller

SL6550 is a system-on-chip NFC controller designed for supporting an NFC communication system embedded in mobile phones, as well as those devices compliant with NFC standards (NFC Forum, NCI, EMVCo, ETSI/SCP).

SL6550 embeds a 13.56MHz contactless front-end supporting three operating modes according to NFC Forum:

- ◆ **Card emulation**
For contactless card functionality, NFC device, such as SL6550, not only can act autonomously if previously configured by the host in such a manner, but also can operate without mobile devices being turned on.
- ◆ **Reader/Writer**
In Reader/Writer mode, an NFC reader interrogates a tag to execute a transaction. NFC Forum defines 5 types of tags, which cover a wide range of applications. The reader can be either a dedicated NFC reader, or a mobile device. An NFC reader is capable of sensing the presence of more than one tag.
- ◆ **Peer-to-peer communication.**
This mode is designed for exchanging data such as contact information between two NFC devices like mobile phones. Each peer takes turn as a reader (transceiver) and tag for a complete exchange between both parties.

In addition, the embedded firmware and associated macrocells of SL6550 support the handling and protocols for the various interfaces:

- ♦ 2 Single Wire Protocol (SWP) interfaces fully compliant with ETSI TS 102 613 specifications
- ♦ I²C Slave interface up to 1 MHz fully compliant with NXP specifications
- ♦ SPI Slave interface up to 4 Mbit/s fully compliant with Freescale specifications

SL6550 can be triggered only by a simple tap; NFC transactions are short, lasting just a fraction of a second, with no need for any preliminary steps. SL6550 also allows to provide a higher output power by supplying the transmitter output stage from 2.7 V to 5.25 V.

Figure 2. shows more detailed transmission mode information supported by SL6550.

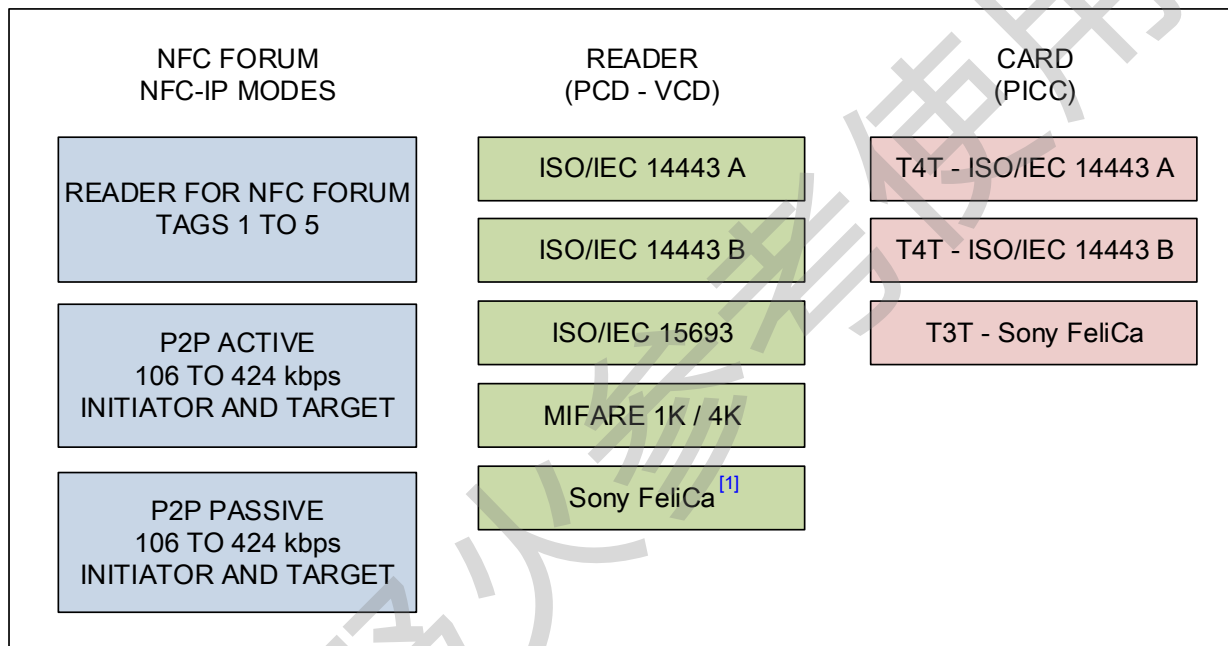


Figure 2. SL6550 transmission modes

3. Key product Features

■ Supported 3 operating modes

- ♦ Reader/Writer Mode
- ♦ Card Emulation Mode
- ♦ Peer-to-Peer Mode

■ Supported RF protocols

- ♦ ISO/IEC 14443A/B PICC mode
- ♦ ISO/IEC 14443A/B PCD mode
- ♦ ISO/IEC 15693 VCD mode
- ♦ FeliCa™ PICC mode
- ♦ FeliCa™ PCD mode
- ♦ MIFARE PCD encryption mechanism (MIFARE 1K/4K)
- ♦ NFCIP-1, NFCIP-2 protocol
- ♦ NFC Forum tags T1T, T2T, T3T, T4T and T5T

- ◆ NFC forum compliant embedded T4T for NDEF short record
- **RF Contactless Front-end**
 - ◆ Integrated RF level detector
 - ◆ Automatic wake-up via RF field detector
 - ◆ Highly integrated demodulator and decoder
 - ◆ Integrated routing mechanism to support multiple NFC execution environments
 - ◆ Integrated Polling Loop for automatic device discovery
 - ◆ Output buffer to connect an NFC antenna with minimum number of external components
- **Supported interfaces**
 - ◆ NCI protocol interface
 - ◆ I2C interfaces in High-speed mode
 - ◆ SPI interfaces
 - ◆ HCI protocol interfaces
 - ◆ Two SWP interfaces
- **System clock**
 - ◆ Support 27.12MHz external crystal oscillator
 - ◆ Integrated PLL unit based on mobile device reference clock
- **Power Management Unit**
 - ◆ Support mobile battery (2.3V~5.5V)
 - ◆ Supply 2 power regulators to UICC in class B and class C
 - ◆ Support multiple low-power strategies
- **Other Features**
 - ◆ Integrated 128KByte eFlash and 8KByte SRAM
 - ◆ Integrated microcontroller
 - ◆ Integrated internal timer
- **Standards compliancy**
 - ◆ NFC Forum Device Requirements v1.3
 - ◆ EMVCo 2.5 for PICC and for PCD mode
 - ◆ ETSI/SCP 102 613 and 102 622 for SWP/HCI
- **Package information**
 - ◆ Package Name: VFBGA64
 - ◆ Package Size: 4.0*4.0*0.85 mm

4. Applications

- Smart-phones
- Portable electronic devices (Wearable, PCs, Gaming Platform, and so on)
- Industrial devices
- Electromedical devices
- Consumer electronic devices

5. Quick reference data

Table 1. Quick reference data

These specification and Pin information of SL6550 were same as PN553.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{BAT}	battery supply voltage	Card Emulation and Passive Target; V _{DD(UP)} > 2.9 V; V _{SS} = 0V	2.5	-	5.5	V
		Reader, Active Initiator and Active Target; V _{DD(UP)} > 3.1 V; V _{SS} = 0V	2.8	-	5.5	V
V _{DD(UP)}	V _{DD(UP)} input supply voltage	Card Emulation and Passive Target; V _{SS} = 0V	2.9	-	5.8	V
		Reader, Active Initiator and Active Target; V _{SS} = 0V	3.1	-	5.8	V
V _{DD(PAD)}	V _{DD(PAD)} supply voltage	supply voltage for host interface; V _{SS} = 0V	1.65	1.8	3.6	V
V _{DD(GPIO)}	V _{DD(GPIO)} supply voltage	supply voltage for GPIO; V _{SS} = 0V	1.65	1.8	3.6	V
V _{DD(SIM_PMU_X)}	UICC input power from external PMU	class C, UICC compliant to ETSI 102 221 rel 9	1.65	-	1.98	V
		class C, UICC compliant to ETSI 102 221 rel 12; I _{VDD(SIM_PMU_X)} = 60mA	1.75	-	1.85	V
		class B; I _{VDD(SIM_PMU_X)} = 50mA	2.91	-	3.3	V
V _{DD(SIM_X)}	UICC power supply	no V _{DD(SIM_PMU_X)} ; I _{VDD(SIM_X)} = 10m	1.625	-	1.98	V
I _{BAT}	battery supply current	in Hard Power Down state; V _{BAT} = 3.6 V; T = 25 °C	-	8.5	-	μA
		in Standby state; V _{BAT} = 3.6 V	-	-	-	-
		enhanced RF detector	-	10.8	-	μA
		in low-power polling loop; V _{BAT} = 3.6 V; T = 25 °C; loop time = 500 ms	-	50	-	μA
		continuous total current consumption in PCD mode at V _{BAT} = 3.6 V	-	-	290	mA
I _{th(Ilim)}	current limit threshold	current limiter on transmitter	270	300	330	mA

Table 1. Quick reference data

These specification and Pin information of SL6550 were same as PN553.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P _{tot}	total power dissipation	PCD mode at typical V _{DD(TX)} = 5.25 V, V _{DD(UP)} = 5.8 V and V _{BAT} = 3.6 V; includes power from V _{BAT} and V _{DD(UP)}	-	-	620	mW
T _{amb}	ambient temperature	JEDEC PCB-0.5	-25	-	+85	°C

[1]. V_{SS} represents V_{SS(PAD)} and V_{SS(TX)}.

[2]. X = 1 or 2.

[3]. External clock on NFC_CLK_XTAL1 must be LOW.

6. Block diagram

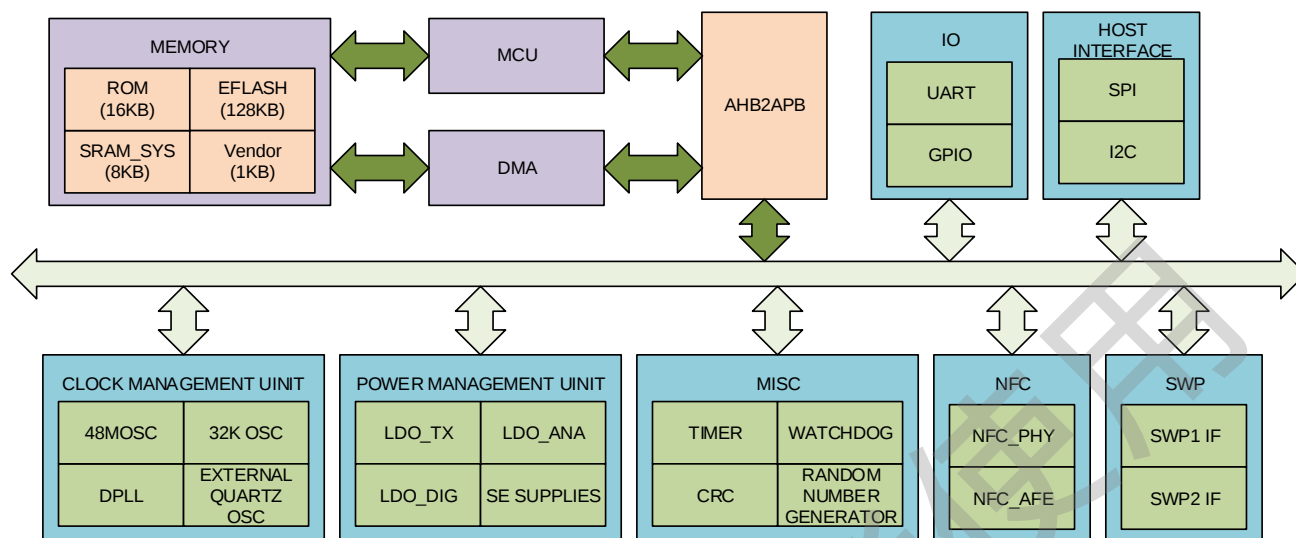


Figure 3. SL6550 block diagram

7. Pinning information

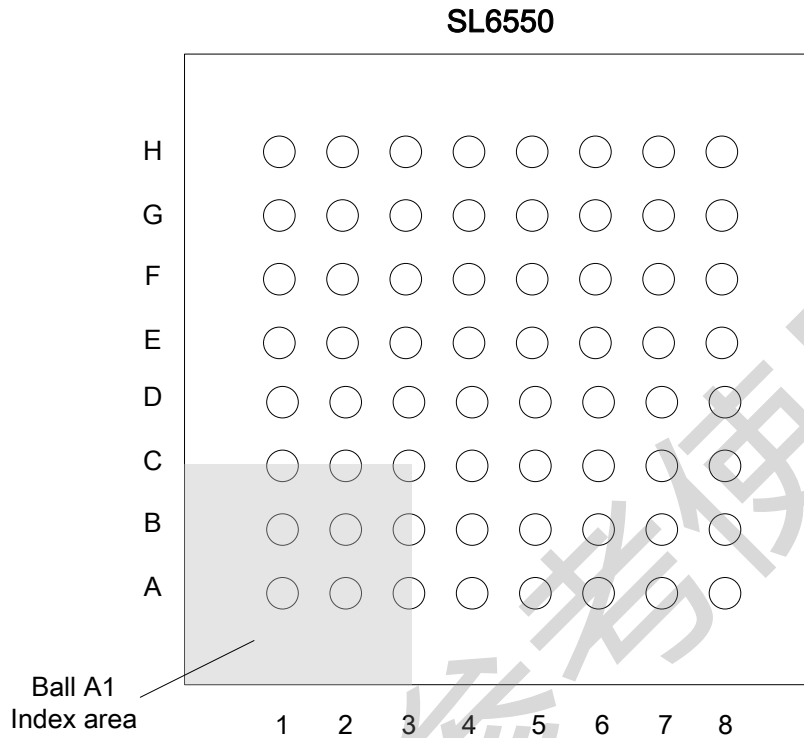


Figure 4. SL6550 pinning (bottom view)

Table 2. SL6550 pin description

Symbol	Pin	Type ^[1]	Refer	Description
WKUP_REQ	A1	I	VDD(PAD)	Wake-up request when in standby
NFC_GPIO_7	A2	I/O	VDD(PAD)	general purpose I/O
SIM_SWIO_1	A3	I/O	VDD or VDD(SIM_PMU_1)	SWP data connection to UICC1. To be left open if not used
VDD(SIM_PMU_1)	A4	P	n/a	UICC1 input power from external PMU
VDD(SIM_1)	A5	P	n/a	UICC1 power supply
SIM_SWIO_2	A6	I/O	VDD or VDD(SIM_PMU_2)	SWP data connection to UICC2. To be left open if not used
VDD(SIM_PMU_2)	A7	P	n/a	UICC2 input power from external PMU
VDD(SIM_2)	A8	P	n/a	UICC2 power supply
CLK_REQ	B1	O	VDD(PAD)	clock request pin
NFC_GPIO_1	B2	I/O	VDD(PAD)	general purpose I/O

Table 2. SL6550 pin description

Symbol	Pin	Type ^[1]	Refer	Description
SIM_IO_PULLDOWN_1	B3	O	VDD(SIM_1)	pull-down for UICC1 IO line
n.c.	B4	-	-	not connected; leave open
n.c.	B5	-	-	not connected; leave open
SIM_IO_PULLDOWN_2	B6	O	VDD(SIM_2)	pull-down for UICC2 IO line
i.c.	B7	-	-	internally connected; leave open
i.c.	B8	-	-	internally connected; leave open
VSS(PAD)	C1	G	n/a	pad ground
NFC_GPIO_0	C2	I/O	VDD(PAD)	general purpose I/O
HIF1	C3	I/O	VDD(PAD)	host interface pin 1
n.c.	C4	-	-	not connected; leave open
n.c.	C5	-	-	not connected; leave open
VSSD	C6	G	n/a	digital ground supply voltage
VDDD	C7	P	n/a	digital supply voltage for decoupling
NFC_CLK_XTAL1	C8	I	VDDD	PLL input
HIF2	D1	I/O	VDD(PAD)	host interface pin 2
VDD(PAD)	D2	P	n/a	pad supply voltage
DWL_REQ	D3	I	VDD(PAD)	firmware download control pin
n.c.	D4	-	-	not connected; leave open
n.c.	D5	-	-	not connected; leave open
VDD(HF)	D6	P	n/a	monitor rectifier output voltage
VDDA	D7	P	n/a	analog supply voltage; connect to VDDD.
XTAL2	D8	O	VDDD	oscillator output
HIF3	E1	I/O	VDD(PAD)	host interface pin 3
HIF4	E2	I/O	VDD(PAD)	host interface pin 4
IRQ	E3	O	VDD(PAD)	interrupt request output
n.c.	E4	-	-	not connected; leave open
n.c.	E5	-	-	not connected; leave open
n.c.	E6	-	-	not connected; leave open
ANT2	E7	P	n/a	antenna connection for wake-up
VBAT	E8	P	n/a	battery supply voltage
NFC_GPIO_6	F1	I/O	VDD(GPIO)	general purpose I/O
NFC_GPIO_3	F2	I/O	VDD(GPIO)	general purpose I/O
NFC_GPIO_2	F3	I/O	VDD(GPIO)	general purpose I/O
n.c.	F4	-	-	not connected; leave open
n.c.	F5	-	-	not connected; leave open
n.c.	F6	-	-	not connected; leave open
ANT1	F7	P	n/a	antenna connection for wake-up

Table 2. SL6550 pin description

Symbol	Pin	Type ^[1]	Refer	Description
TX_PWR_REQ	F8	O	VDDD	external TX power supply request on VDDD
VDD(GPIO)	G1	P	-	general purpose I/O supply voltage
NFC_GPIO_5	G2	I/O	VDD(GPIO)	general purpose I/O
VSSA	G3	G	n/a	analog ground supply voltage
n.c.	G4	-	-	not connected; leave open
VSSA	G5	G	n/a	analog ground supply voltage
VSSA	G6	G	n/a	analog ground supply voltage
VDD(TX)	G7	P	n/a	transmitter supply voltage
TX1	G8	O	VDD(TX)	antenna driver output
VEN	H1	I	VBAT	reset pin. Set the device in Hard Power Down
NFC_GPIO_4	H2	I/O	VDD(GPIO)	general purpose I/O
VDD(UP)	H3	P	n/a	TXLDO input supply voltage
VDD(MID)	H4	P	n/a	receiver reference input supply voltage
RXP	H5	I	VDDA	positive receiver input
RXN	H6	I	VDDA	negative receiver input
TX2	H7	O	VDD(TX)	antenna driver output
VSS(TX)	H8	G	n/a	contactless transmitter ground

[1]. P = power supply; G = ground; I = input, O = output; I/O = input/output.

8. Functional description

SL6550 is connected with host controller through host interface. Either SPI-bus or I²C-bus can be selected as the host interface. The host interface is NCI-compliant.

2 SWP secure element can be connected with SL6550 at the same time and can work independently.

A 128KB EFLASH is provided to support firmware updating.

Ultra low power is guaranteed by a powerful integrated power management unit(PMU). Hard Power Down, Standby and Active mode are supported by PMU.

Figure 5 shows the connection of SL6550 in mobile system.

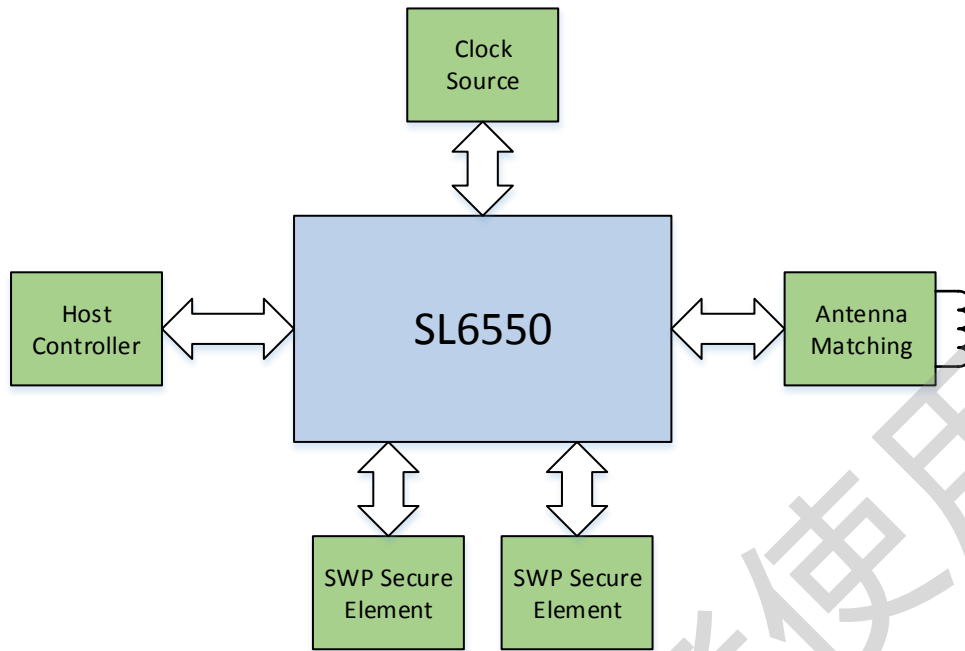


Figure 5.SL6550 connection in mobile system

8.1 System mode

8.1.1 Power states

SL6550 defined 4 power states: Power Off, Hard Power Down(HPD), Standby and Active.

- **Power Off:**
The SL6550 is not supplied from any source.
- **Hard Power Down:**
The SL6550 is supplied by V_{BAT} within its operating range and V_{EN} is kept low by host(or by SW programming when $V_{DD(PAD)}$ is not supplied). In this state, SL6550 has the minimum power consumption, all registers and internal states are reset.
- **Standby:**
The SL6550 is supplied by V_{BAT} within its operating range and V_{EN} is kept high by host(or by SW programming when $V_{DD(PAD)}$ is not supplied), system power state is switch into this state by internal MCU or by host through host interface. In this state, minimum part of SL6550 is supplied. All enabled wakeup source are allowed to switch SL6550 into Active state.
- **Active:**
The SL6550 is supplied by V_{BAT} within its operating range and V_{EN} is kept high by host(or by SW programming when $V_{DD(PAD)}$ is not supplied). This is the default state after chip power on. The entire chip is supplied in this state.

SL6550 will automatically switch power state at application level to optimize power consumption. Also, host controller has full control of SL6550 and can specify the state of SL6550 directly.

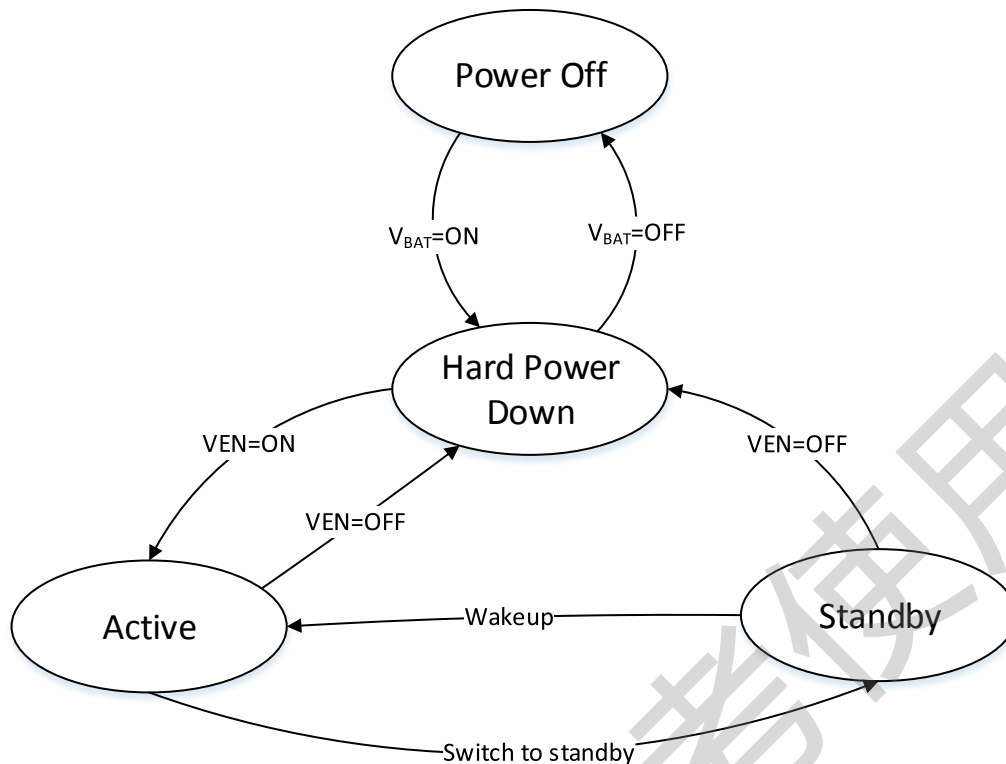


Figure 6.power states transition

8.1.1.1 Hard Power Down state

The Hard Power Down state is entered when V_{BAT} is supplied and VEN pin voltage is below 0.3V. When $V_{DD(PAD)}$ is supplied, host is supposed to keep VEN low to keep SL6550 staying in HPD state. In some cases, $V_{DD(PAD)}$ is powered off to reduce power consumption and VEN pin is unable to be kept low. An internal register “VEN_reg” is provided to handle this. Set this register to 0 can hold HPD state when $V_{DD(PAD)}$ is powered off. When $V_{DD(PAD)}$ is supplied, “VEN_reg” is ignored.

Table 3. VEN value used by SL6550

$V_{DD(PAD)}$	VEN PIN	VEN_reg	VEN(internal used)
On	1	x	1
On	0	x	0
Off	x	1	1
Off	x	0	0

8.1.1.2 Standby state

Standby state is used to reduce power consumption. In this state, V_{BAT} is supplied and internal used VEN value is supposed to be high(that means VEN pin is high when $V_{DD(PAD)}$ is supplied and VEN_reg is high when $V_{DD(PAD)}$ is off). Most parts of SL6550 are powered off in this state. Several wakeup sources can be used to switch SL6550 into Active state(all host-related wakeup imply that $V_{DD(PAD)}$ is available):

- Host interface wakeup event(I²C-bus, SPI-bus)
- Host interface wakeup via WKUP_REQ pin
- Antenna RF level detector
- Internal timer event

- UICC SWP interface over $V_{DD}(\text{SIM_PMU_1})$, $V_{DD}(\text{SIM_PMU_2})$, SIM_SWIO_1 or SIM_SWIO_2
- Polling loop card detected or RF level detected event

If any of above wakeup event occurs, SL6550 will switch into Active state. Any further operation depends on software configuration.

8.1.1.3 Active state

SL6550 act as an NFC device within Active state. 3 sub states are defined in Active state: Active.Idle, Active.Poller and Active.Listener.

- Active.Idle state:
SL6550 is in Active state and waiting for further host interface communication. The RF interface is not activated. SL6550 is switching into this state once wakeup from Standby state.
- Active.Poller state:
In Active.Poller state, the RF interface is activated. SL6550 is acting as Reader/Writer or NFC Initiator, searching for or communicating with passive tags or NFC target.
Active.Poller state shall be used with $2.8\text{V} < V_{\text{BAT}} < 5.5\text{V}$ and $\text{VEN voltage} > 1.0\text{V}$.
- Active.Listener state:
SL6550 acts as a card or an NFC Target in this state. Active.Listener state shall be used with $2.8\text{V} < V_{\text{BAT}} < 5.5\text{V}$ and $\text{VEN voltage} > 1.0\text{V}$.

8.1.2 Polling loop

SL6550 periodically polls external devices and listen to external RF signals. This is called polling loop. 3 phases are defined in polling loop: polling phase, listening phase and pause phase. An entire polling loop usually consist of a polling phase and a listening phase, or a polling phase and a pause phase, depending on whether card emulation is needed. In pause phase, SL6550 has nothing to do.

8.1.2.1 Standard polling loop

In listening phase, if no RF signal is detected, SL6550 stays in Standby state or Active.Idle state, depends on the configuration. Once RF signal is detected, SL6550 switches into Active.Listener state and exits polling loop.

In polling phase, SL6550 polls external device with all supported RF command sequentially. Once NFC Target or card/tag present, SL6550 switches into Active.Poller state and exits polling loop.

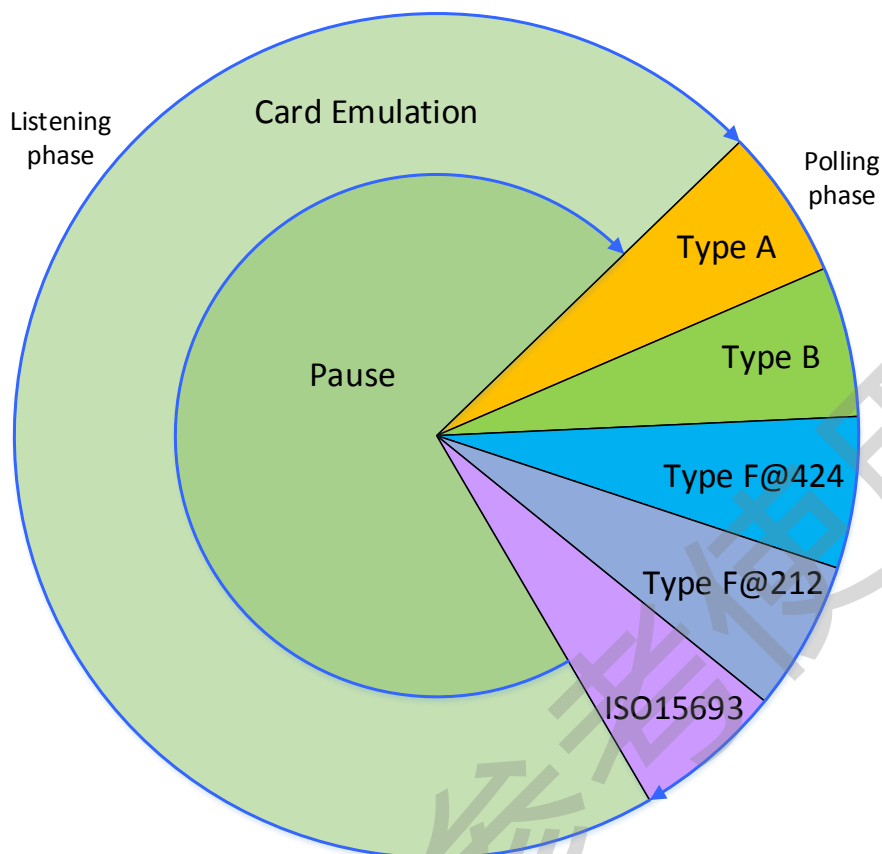


Figure 7. Standard polling loop

8.1.2.2 Low power polling loop

Low power polling loop is introduced to decrease power consumption. Sending a short duration of RF field is used instead of sending RF command. If there is any NFC target or card/tag present, SL6550 can detect it through the changing of field strength. With 500ms polling duration, the average power consumption is about 20uA~50uA, depends on the polling configuration and the antenna matching.

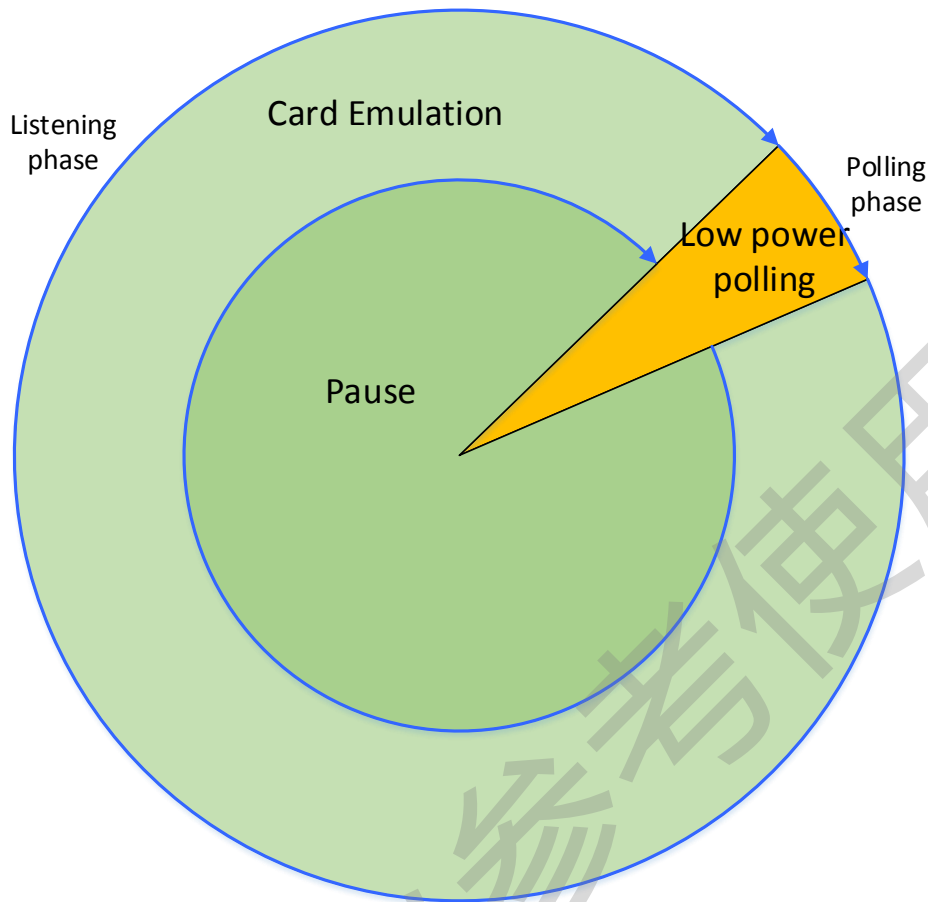


Figure 8.Low power polling loop

8.2 Host interface

SL6550 provide 2 types of host interface, SPI-bus and I²C-bus. Only one host interface can be used at the same time since they share the same pins. The host interface type can be selected by EFLASH programming which is done during IC manufacturing.

Besides SPI-bus and I²C-bus, an extra pin is provided as the IRQ from SL6550 to host controller to enable the data flow control between SL6550 and host.

8.2.1 I²C-bus interface

I²C-bus features are listed below:

- Support slave I²C-bus
- Support up to 3.4M baud rate.
- Support wakeup on I²C address
- Support clock stretching(SL6550 can hold SCL low as a handshake with host controller to suspend and resume I²C transfer)

When I²C-bus is selected in the EFLASH, HIF1, HIF2, HIF3 and HIF4 are mapped to I²C functionality, which is described in Table 4.

Table 4. Functionality mapping when configured as I²C-bus

Pin name	Functionality
----------	---------------

HIF1	I ² C-bus address 0
HIF2	I ² C-bus address 1
HIF3	I ² C-bus data line SDA
HIF4	I ² C-bus clock line SCL

HIF3 and HIF4 are used as the I²C-bus data line and clock line.

I²C address is determined by the value of HIF1 and HIF2, the address mapping is described in Table 5.

Table 5. I²C-bus addressing

HIF2	HIF1	I ² C-bus address (R/W = 0, write)	I ² C-bus address (R/W = 1, read)
0	0	0x50	0x51
0	1	0x52	0x53
1	0	0x54	0x55
1	1	0x56	0x57

8.2.2 SPI-bus interface

SPI-bus features are listed below:

- Support SPI-bus slave mode
- Support up to 10Mbps
- Support full-duplex communication
- Support programmable clock polarity(CPOL) and clock phase(CPHA)
- Support wakeup on transition of NSS

When SPI-bus is selected in the EFLASH, HIF1, HIF2, HIF3 and HIF4 are mapped to SPI functionality, which is described in Table 6.

Table 6. Functionality mapping when configured as SPI-bus

Pin name	Functionality
HIF1	NSS(slave select, low active)
HIF2	MOSI(master out slave in)
HIF3	MISO(master in slave out)
HIF4	SCK(serial clock)

CPOL and CPHA are programmed during IC manufacturing.

CPOL description:

- If CPOL = 0: SCK is low when SPI-bus is idle, and the first valid edge of SCK will be a rising edge.
- If CPOL = 1: SCK is high when SPI-bus is idle, and the first valid edge of SCK will be a falling edge.

CPHA description:

- If CPHA = 0: MOSI data are sampled by SL6550 at the odd edges of SCK after NSS goes low.
- If CPHA = 1: MOSI data are sampled by SL6550 at the even edges of SCK after NSS goes low.

In SL6550, both on MOSI line and MISO line, data are required to be sent with the most significant bit(MSB) first.

To be compatible with other SPI devices, MISO line can be set to high impedance when SL6550 is not selected by host controller via NSS.

8.3 Secure element interface

2 single wire protocol(SWP) interfaces are provided to be connected to secure element and they are ETSI HCI compliant.

SL6550, acting as the contactless front end, communicates with secure element via SWP interface. SL6550 is the master and the secure element is the slave. SWP interface is a full-duplex interface. The master sends data on the wire in the voltage domain, and the slave sends data back in the current domain.

There are two SWP interfaces. Since they are physically individual, the two SWP interfaces can be active at the same time.

8.3.1 UICC SWP interface

The 2 SWP interfaces in SL6550 are:

- SIM_SWIO_1, which is supplied by $V_{DD(SIM_1)}$. When $V_{DD(SIM_PMU_1)}$ is available, $V_{DD(SIM_1)}$ comes from $V_{DD(SIM_PMU_1)}$, or it comes from internal regulator.
- SIM_SWIO_2, which is supplied by $V_{DD(SIM_2)}$. When $V_{DD(SIM_PMU_2)}$ is available, $V_{DD(SIM_2)}$ comes from $V_{DD(SIM_PMU_2)}$, or it comes from internal regulator.

The 2 SWP interfaces support both classes B and C depending on the power supply.

The interface data rate support 1.7Mbps/910kbps. 910kbps is the default data rate, while 1.7Mbps is activated by firmware if the secure element supports it.

SL6550 also allows configuration of SIM_SWIO_1 and SIM_SWIO_2 pins in high impedance state.

Capacitance connected with SIM_SWIO_1 and SIM_SWIO_2 should not exceed the maximum capacitance load specified in Table 7 to guarantee maximum baudrate for SWP communication towards ETSI-compliant UICCs.

Table 7. SWIO capacitance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Csim_swio_load	maximum SWIO capacitance load		-	-	66	pF

8.4 Wakeup from standby

Multiple wakeup sources are provided in SL6550. Each source can be configured enable or disable individually. Wakeup sources are listed below:

- I²C-bus event wakeup
When I²C address matches SL6550 I²C slave address then trigger I²C-bus event and wakeup.
- SPI-bus event wakeup
SPI-bus event occurs when NSS high, NSS low or NSS change, depends on SW configuration.
- WKUP_REQ pin wakeup

SL6550 is woken up when WKUP_REQ high, WKUP_REQ low or WKUP_REQ change, depends on SW configuration.

- Antenna RF level detector wakeup

An Antenna RF level detector is used to detect the external RF signals. Depends on the configuration, this detector generate wakeup signal when RF signals are detected or RF signals disappeared.

- Internal timer event wakeup

Specific time can be set to the internal timer. A wakeup signal is generated at timer counter underflow.

- UICC SWP1 and UICC SWP2 interface power supply detector wakeup

Voltage of $V_{DD}(SIM_PMU_1)$ and $V_{DD}(SIM_PMU_2)$ are monitored. 2 thresholds, 0.65V and 2.4V are set for the detectors so SL6550 can distinguish 1.8V power supply and 3.3V power supply. Once the power status changes, a wakeup signal is generated.

- UICC SWP1 and UICC SWP2 interface resume wakeup

When UICC resume from SE is detected, a wakeup signal is generated.

- Polling loop event wakeup

In polling loop, if any external device is detected, a wakeup signal is generated.

When SL6550 is woken up by any of the wakeup sources, T_{boot} is needed before host communication.

To reduce the time cost at wakeup, fastboot option is provided. When fastboot is enabled, $T_{fastboot}$ is needed instead of T_{boot} before host communication.

8.5 Clock Introduction

There are 4 different clock sources in SL6550:

- 27.12MHz clock used for RF communication, which comes from:
 - Internal oscillator with external crystal connection on NFC_CLK_XTAL1 and XTAL2 pins.
 - External reference clock on pin NFC_CLK_XTAL1.
 - Internal DPLL when external crystal is not 27.12MHz or external reference clock is not 27.12MHz.
- 13.56MHz clock recovered from RF field.
- 40MHz system clock from low-power internal oscillator.
 - With $\pm 2.5\%$ accuracy.
- 32KHz PMU clock from low-power internal oscillator.
 - Low frequency oscillator used to drive PMU and related wakeup circuit.

8.5.1 27.12MHz quartz oscillator

When enabled, the 27.12MHz quartz oscillator offers the reference clock for SL6550 when it behaves in Reader mode or NFCIP-1 Initiator.

The recommended circuit is shown in following Figure 9.

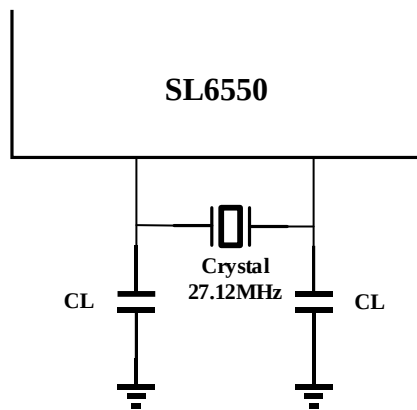


Figure 9. 27.12MHz crystal oscillator connection

The following table describes the accuracy and stability requirement of the crystal.

Table 8. Crystal requirement

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F _{xtal}	Crystal frequency	ISO/IEC, FCC and Felica global compliancy	-	27.12	-	MHz
ΔF _{xtal}	Crystal frequency accuracy	Full operating range	-50	-	+50	ppm
ESR	Equivalent series resistance		-	50	100	Ω
CL	Load capacitance		-	10	-	pF
P _{xtal}	Crystal power dissipation		-	-	100	μW

8.5.2 DPLL to generate 27.12MHz clock

The integrated Sigma-Delta DPLL is used to generate a low noise 27.12MHz clock, the input clock frequency of DPLL is covered a continuously range from 19.2MHz to 48MHz.

The input clock on NFC_CLK_XTAL1 should meet the following phase noise requirement:

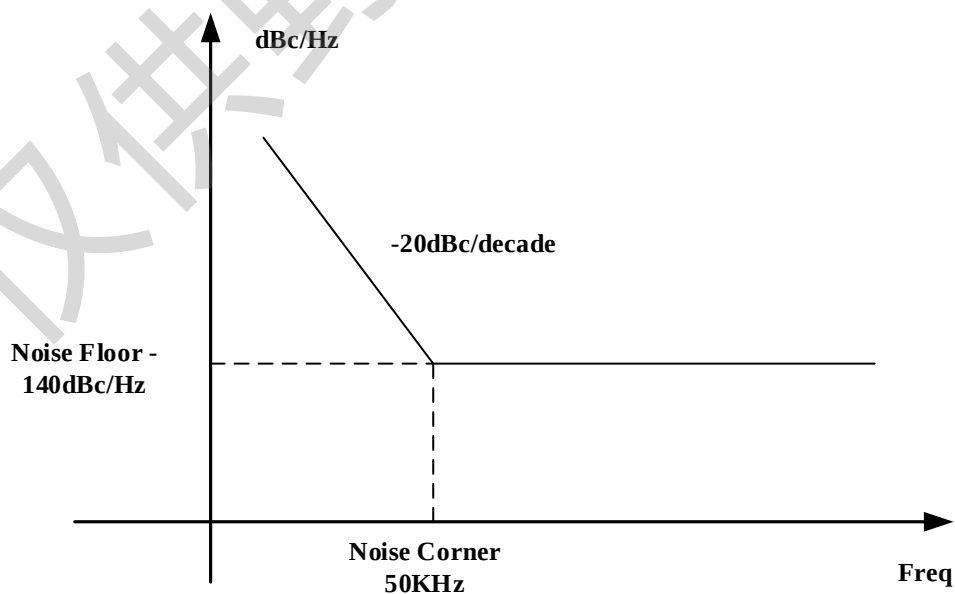


Figure 10. Input reference phase noise characteristics

The following table describes the requirement of input clock on NFC_CLK_XTAL1.

Table 9. DPLL input requirement

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{clk}	Clock Frequency	ISO/IEC, FCC and Felica global compliancy	19.2	-	48	MHz
$F_{i(ref)acc}$	Input frequency accuracy	-	-20	-	20	ppm
Φ_n	Phase noise	Noise corner at 50kHz	-140	-	-	dBc/Hz
Sinusoidal shape						
$V_{i(p-p)}$	Peak-to-peak input voltage	-	0.2	-	1.8	V
$V_{i(clk)}$	Clock input voltage	-	0	-	1.8	V
Square shape						
$V_{i(clk)}$	Clock input voltage	-	0	-	1.8	V

8.6 Power Supply

8.6.1 Power functional description

SL6550 needs 6 external power supply as follows:

- VDD_GPIO: GPIO Power Supply, 1.8V or 3V
- VDD_PAD: PAD Power Supply, 1.8V or 3V
- VBAT: Supply from Battery
- VDD(UP): Supply Power for LDO_TVDD, it can be either connected to VDD(UP) or VBAT
- VDD(SIM_PMU_1): Main Power for UICC1, 0V 1.8V or 3V
- VDD(SIM_PMU_2): Main Power for UICC2, 0V 1.8V or 3V

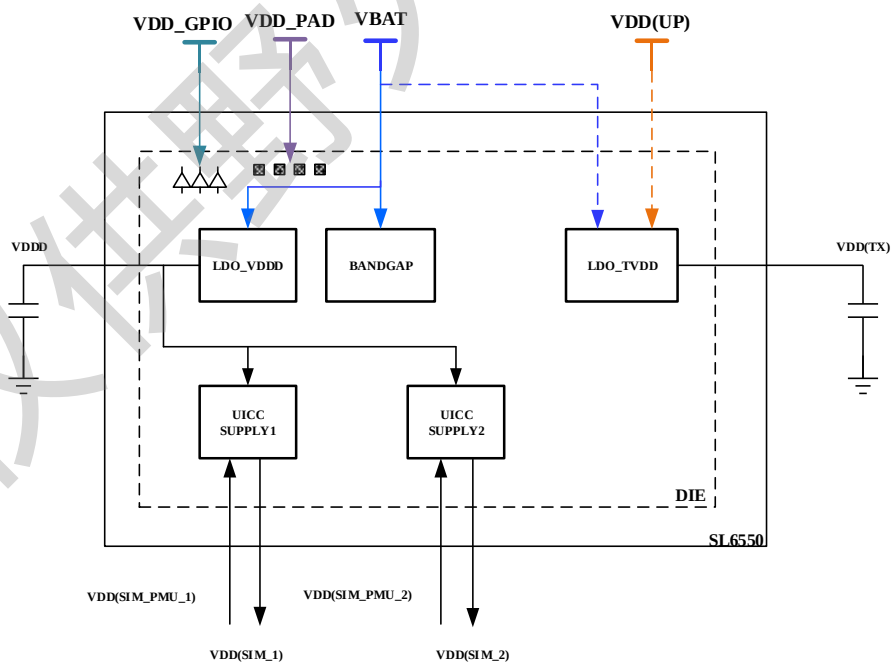


Figure 11. Power functional diagram

SL6550 generate 4 internal power as follows:

- VDDD: Power supply for digital part generate from LDO_VDDD
- VDD(TX): Power supply for TX part generate from LDO_TVDD
- VDD(SIM_1): Power supply for UICC1
- VDD(SIM_2): Power supply for UICC2

8.6.2 LDO_VDDD

The input pin of LDO_VDDD is VBAT.

The output voltage of LDO_VDDD is VDDD 1.8V, it must be de-coupled with external capacitor.

8.6.3 LDO_TVDD

Transmitter voltage is generated by integrated LDO_TVDD.

This LDO_TVDD can offer a maximum continuous current load up to 250mA in order to support ISO/IEC 14443, EMVCo and NFC Forum standard compliant operations.

The output voltage of LDO_TVDD can be configured, and it's output pin must be de-coupled with external capacitor.

Table 10. LDO_TVDD

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD(LDO_TVDD)(drop)	Drop of LDO_TVDD supply voltage	VDD(UP)=5.3V; Transmitter current =250mA	-	-	0.3	V

The power supply of LDO_TVDD can be configured in two mode.

8.6.3.1 Mode 1: The battery voltage is the power supply of LDO_TVDD

The input pin of LDO_TVDD named VDD(UP) is directly connected to the battery voltage on the PCB board.

The output pin of LDO_TVDD named VDD(TX).

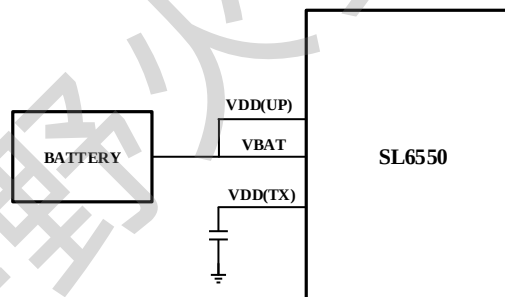


Figure 12. VDD(UP)=VBAT(between 2.8V and 5.5V)

8.6.3.2 Mode 2: An external voltage is the power supply of LDO_TVDD

In this mode, VDD(UP) is powered by EXTERNAL SUPPLY. The EXTERNAL SUPPLY may be a BOOST-DCDC or other device powered by BATTERY voltage VBAT.

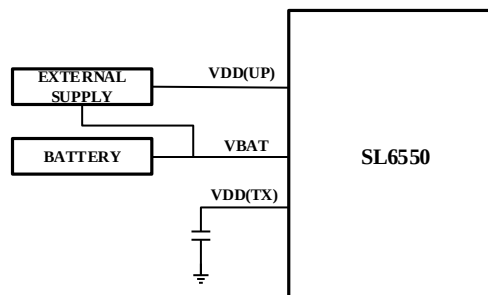


Figure 13. VDD(UP) generate from EXTERNAL SUPPLY

8.6.3.3 VDD(TX) Output Voltage Config

LDO_TVDD can output 12 different voltage from 2.5V to 5.2V. To make sure it can work in a heavy load current mode, the input power supply VDD(UP) must be higher than output voltage VDD(TX).

8.6.3.3.1 VD-VDD(UP) Threshold

SL6550 integrates a inner Voltage-Detector: VD-VDD(UP). This circuit monitors VDD(UP) in real-time and quantify the value. The output value of VD-VDD(UP) guide the LDO_TVDD to output proper voltage. VD-VDD(UP) has 0000 to 1111 totally 16 steps to quantify the value of VDD(UP). When VDD(UP) power up, VD-VDD(UP) change control bits from 1111 to 0000, the 1 bit output will generate a thermometer code. Judging from the VD-VDD(UP) output, the proper output voltage of LDO_TVDD can be got.

Table 11. Threshold of VD-VDD(UP)

VTH	VDD(UP) Range (V)	VTH	VDD(UP) Range (V)
1111	6.05~5.95	0111	3.95~3.85
1110	5.8~5.7	0110	3.65~3.55
1101	5.55~5.45	0101	3.35~3.25
1100	5.3~5.2	0100	3.05~2.95
1011	5.05~4.95	0011	2.75~2.65
1010	4.8~4.7	0010	2.55~2.45
1001	4.55~4.45	0001	2.3~2.2
1000	4.25~4.15	0000	2.05~1.95

Every VTH control bit gets 100mV hysteresis range. If VDD(UP) is 4.9V: VTH=1111~1011 the output of VDD(UP) will be '0'; VTH=1010~0000 the output of VDD(UP) will be '1'.

8.6.3.3.2 LDO_TVDD Output Voltage

The output of LDO_TVDD.

The following table show the output value of LDO_TVDD that can be configured by register.

Table 12. Output value of LDO_TVDD

LDO_TVDD Mode	Register Setting	LDO_TVDD_VTH<3:0>	LDO_TVDD Output Voltage (V)
LDO	EN=1MODE=0	1111~1100(not used)	-
		1011	5.2
		1010	5.0
		1001	4.75
		1000	4.7
		0111	4.5
		0110	4.2
		0101	3.9
		0100	3.6
		0011	3.3
		0010	3.0

		0001	2.7
		0000	2.5
SWITCH	EN=1MODE=1	0000~1011	VDD_UP-Iload*Ron

LDO_TVDD works in two mode: LDO and SWITCH.

In LDO mode, LDO_TVDD works on traditional Low-Drop-Out Mode, as long as the input voltage of LDO_TVDD is high enough, the output of LDO_TVDD named VDD(TX) is steady; in SWITCH mode, the LDO_TVDD transfer VDD(UP) voltage to VDD(TX) with a voltage drop of Iload*Ron, Iload is the current load of LDO_TVDD, Ron is the resister of switch.

The two mode of LDO_TVDD is shown as following Figure.

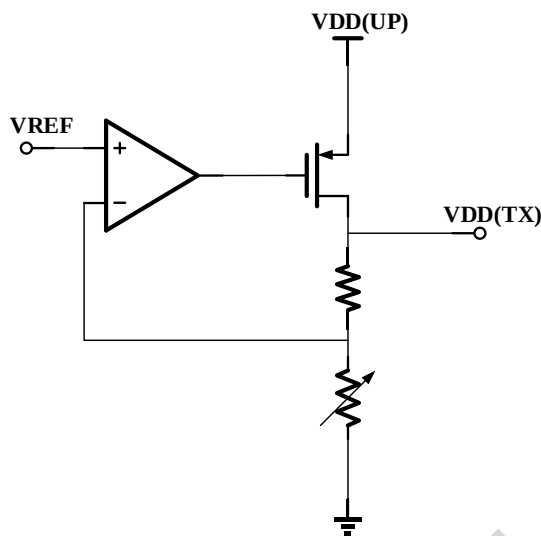


Figure 14. LDO_TVDD LDO-MODE

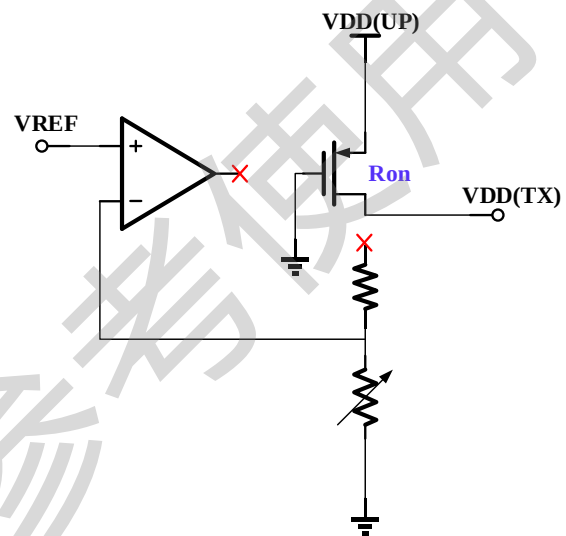


Figure 15. LDO_TVDD SWITCH-MODE

8.6.3.3.3 Co-Work of VD_VDD(UP) and LDO_TVDD

To keep SL6550 emit a large field signal, LDO_TVDD should be configured to the highest output voltage allowed.

The highest output voltage of LDO_TVDD that can be configured is depending on the output of VD_VDD(UP) who monitor the VDD(UP) in real time.

For example VDD(UP) is 5.1V, VD_VDD(UP) output will be 0000 1111 1111 1111 when it's vth configured from 1111 to 0000. The allowed highest output of LDO_TVDD will be 4.7V, the control bits LDO_TVDD_VTH<3:0> is 1000.

The following table shows the relationship between VD_VDD(UP) result and LDO_TVDD output voltage.

Table 13. Relationship between VD_VDD(UP) result and LDO_TVDD output voltage

VD_VDD(UP) Range (V)	VD_VDD(UP): VTH<15:0> Output	LDO_TVDD All Allowed Output (V)	LDO_TVDD Highest Output (V)
VDD(UP)>5.95	1111 1111 1111 1111	2.5~5.2	5.2
5.7<VDD(UP)<5.95	0111 1111 1111 1111	2.5~5.2	5.2
5.45<VDD(UP)<5.7	0011 1111 1111 1111	2.5~5.2	5.2
5.2<VDD(UP)<5.45	0001 1111 1111 1111	2.5~5.0	5.0
4.95<VDD(UP)<5.2	0000 1111 1111 1111	2.5~4.7	4.7

4.7<VDD(UP)<4.95	0000 0111 1111 1111	2.5~4.5	4.5
4.45<VDD(UP)<4.7	0000 0011 1111 1111	2.5~4.2	4.2
4.15<VDD(UP)<4.45	0000 0001 1111 1111	2.5~3.9	3.9
3.85<VDD(UP)<4.15	0000 0000 1111 1111	2.5~3.6	3.6
3.55<VDD(UP)<3.85	0000 0000 0111 1111	2.5~3.0	3.0
3.25<VDD(UP)<3.55	0000 0000 0011 1111	2.5~2.7	2.7
2.95<VDD(UP)<3.25	0000 0000 0001 1111	2.5	2.5
2.65<VDD(UP)<2.95	0000 0000 0000 1111	SWITCH_Mode	VDD(UP)-Iload*1Ω
2.45<VDD(UP)<2.65	0000 0000 0000 0111	SWITCH_Mode	VDD(UP)-Iload*1Ω
2.2<VDD(UP)<2.45	0000 0000 0000 0011	SWITCH_Mode	VDD(UP)-Iload*1Ω
1.95< VDD(UP)<2.2	0000 0000 0000 0001	SWITCH_Mode	VDD(UP)-Iload*1Ω
VDD(UP)<1.95	0000 0000 0000 0000	SWITCH_Mode	VDD(UP)-Iload*1Ω

VDD(UP) higher than 2.95V, LDO_TVDD work on LDO_Mode; VDD(UP) lower than 2.95V, LDO_TVDD works on SWITCH_Mode. When LDO_TVDD works on SWITCH_MODE, the output voltage is $VDD(UP)-Iload*1\Omega$, Iload is load current of LDO_TVDD, 1Ω is the on-resistance of LDO_TVDD.

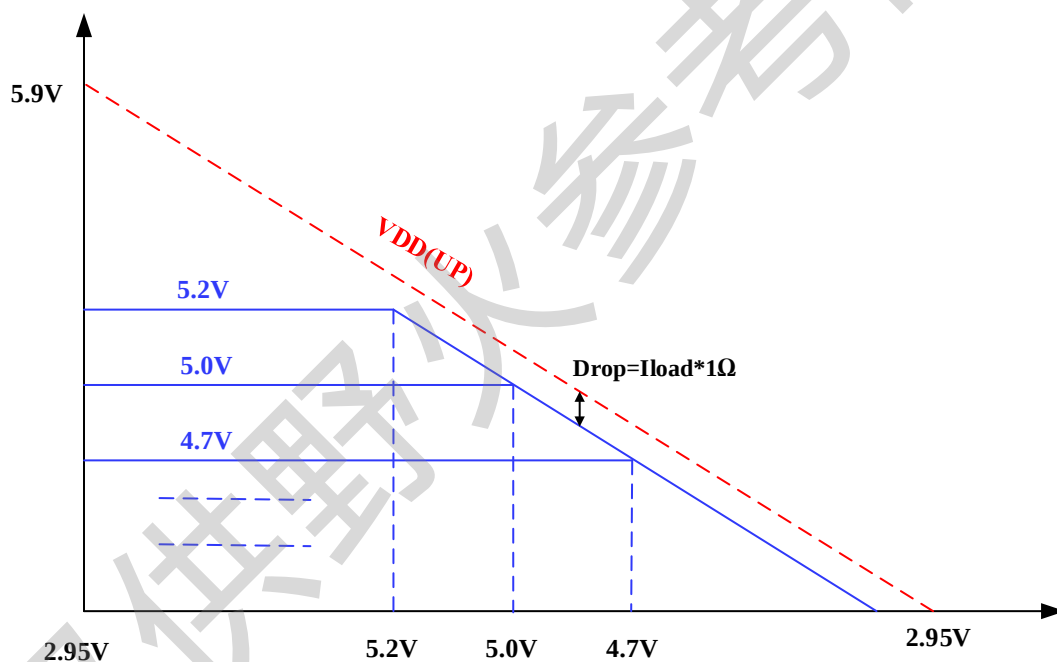


Figure 16. Behavior of LDO_TVDD

8.6.3.4 LDO_TVDD Limiter

The SL6550 integrates a current limiter named IDET to avoid high current within TX1 and TX2.

The IDET compare an image of LDO_TVDD output current to a reference, when the reference is reached the output current of LDO_TVDD get limited.

The limiting current is $300mA \pm 30mA$, above the specified maximum current allowed for RF operation (250mA).

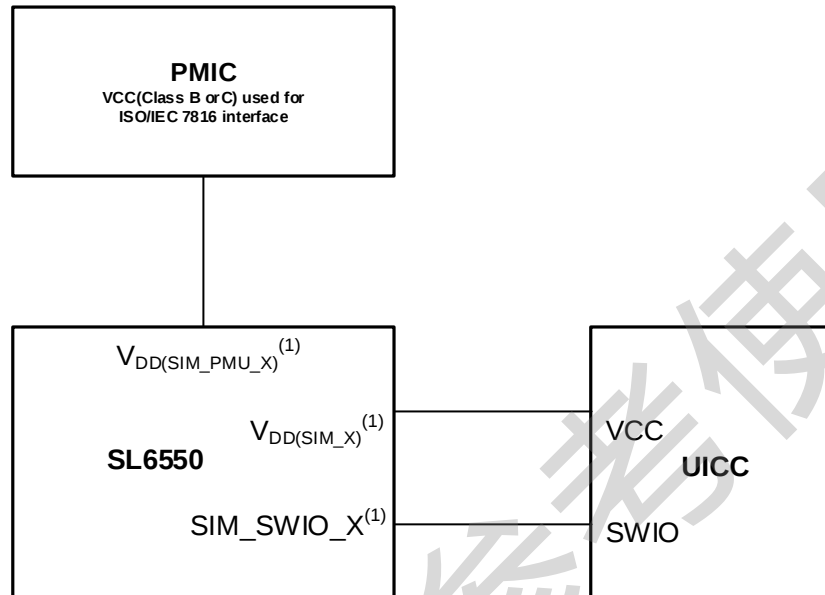
8.6.4 SWP supplies management

The SWP supply blocks are in charge of to deliver the proper supplies for the 2 external SWP devices and also to provide reference supplies for SIM_SWIO_1 and SIM_SWIO_2 data signal.

8.6.4.1 Case of SWP UICC working with mobile switched OFF

In case the SWP connected device is a UICC, to allow the Card Emulation functionality when the mobile device is switched OFF then:

- The UICC connected on SIM_SWIO_X(with X=1 or 2) shall be powered via $V_{DD(SIM_X)}$
- $V_{DD(SIM_PMU_X)}$ shall be connected to the PMU/LDO which is used as reference for the ETSI/SCP 102 221 interface



(1) With X=1 or 2

Figure 17. SWP UICC working with mobile switched OFF

$V_{DD(SIM_X)}$ voltage is present as soon as the PMU/LDO voltage is present and it is of the same class than $V_{DD(SIM_PMU_X)}$. SL6550 withstands 1.8V (class C) or 3V (class B).

When using $V_{DD(SIM_X)}$ (with X=1 or 2) to supply the SWP device with $V_{DD(SIM_PMU_X)}$ connected to an external PMU/LDO:

- If the PMU/LDO is disabled, then a switch has been added to derive $V_{DD(SIM_X)}$ from V_{DDD} , internal 1.8V supply, so that the SL6550 can still supply the UICC. When $V_{DD(SIM_PMU_X)}$ is OFF, $V_{DD(SIM_X)}$ is only high when activity is required on SIM_SWIO_X
- If the PMU/LDO is enabled then $V_{DD(SIM_X)}$ is derived from $V_{DD(SIM_PMU_X)}$

In whatever mode the SL6550 is, including Hard Power Down (V_{EN} voltage < 0.3V), when $V_{DD(SIM_PMU_X)}$ rises, $V_{DD(SIM_X)}$ will follow $V_{DD(SIM_PMU_X)}$.

The SL6550 is able to detect if $V_{DD(SIM_PMU_X)}$ is ON or OFF and from which class it is.

The On resistance of the internal switch between $V_{DD(SIM_PMU_X)}$ and $V_{DD(SIM_X)}$ is designed to be below 1.2ohm in class B and below 1.2ohm in class C.

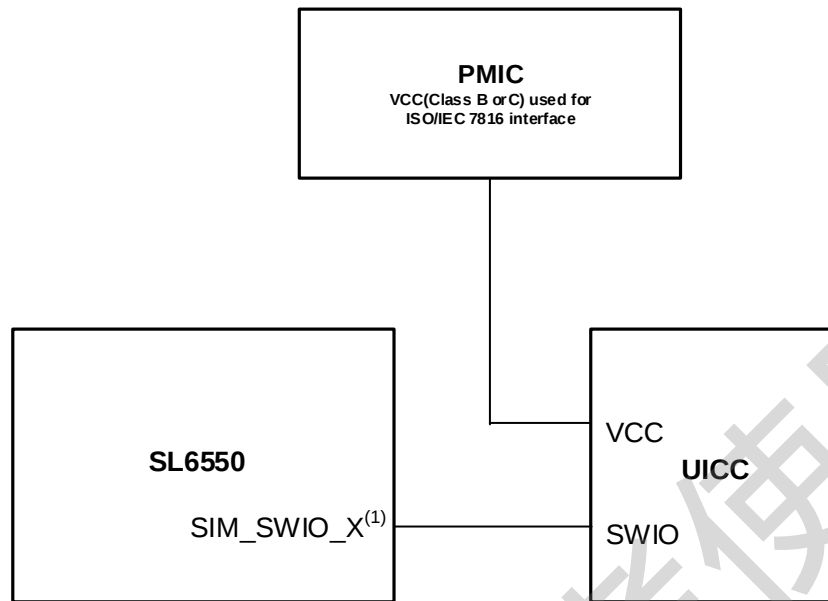
8.6.4.2 Case of SWP UICC working with mobile switched ON

In order to guarantee the compatibility of the SIM_SWIO_1 and SIM_SWIO_2 signals with the specification, the supplies of the connected SWP secure elements shall be compliant with Vcc pin class B or class C.

The SWP device is directly connected to a PMU/LDO. If the SWP secure elements is connected to:

- SIM_SWIO_1 then its Vcc supply shall be connected to $V_{DD(SIM_PMU_1)}$
- SIM_SWIO_2 then its Vcc supply shall be connected to $V_{DD(SIM_PMU_2)}$

This is in order to guarantee the compatibility of the SIM_SWIO_X signal with the specification for both 1.8V (class C) or 3V(class B).



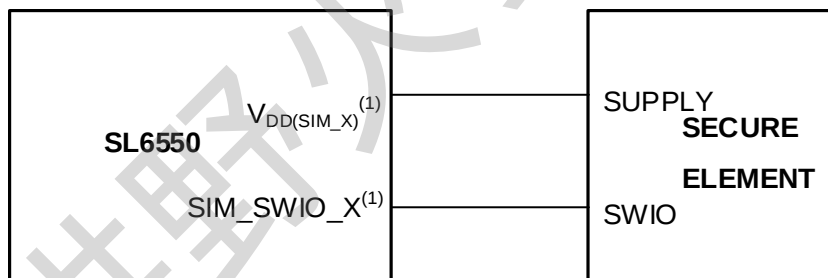
(1) With X=1 or 2

Figure 18. SWP UICC working with mobile switched ON

SL6550 integrate an internal 1.8VLDO to drive the SIM_SWIO_X.

8.6.4.3 Case of non UICC SWP devices working with mobile switched OFF

At the mobile device level, the supply of SWP device supply might be connected to either SL6550 VDD(SIM_X) pins (with X=1 or 2).



(1) With X=1 or 2

Figure 19. SWP devices working with mobile switched OFF

8.7 Reset and download

SL6550 is reset via power on reset, VEN pin or host command. All the reset methods reset the entire SL6550 chip, except that the value of fastboot option is kept when reset by host command.

When been reset, SL6550 MCU stops execution and all register value return to default value. Part of the default values are defined in the EFLASH while others are hardware defined.

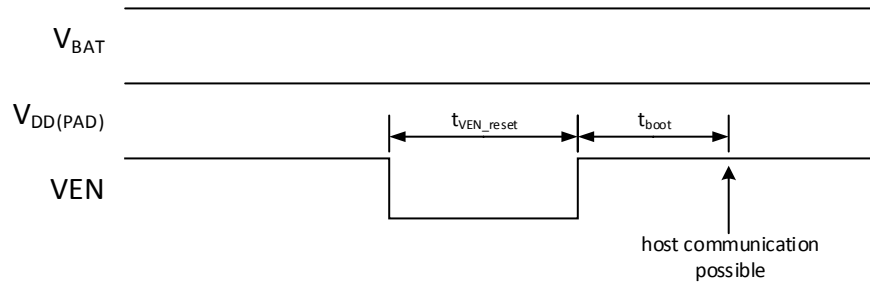


Figure 20.Reset via VEN

8.7.1 Power up sequences

SL6550 allows VEN been controlled by host controller or tie high at board level. Thus different power up sequences is defined.

8.7.1.1 VEN tie high at board level

As VEN is tied high at board level, SL6550 start booting when power is supplied. Built-in power on reset(POR) circuit do resetting to internal circuits.

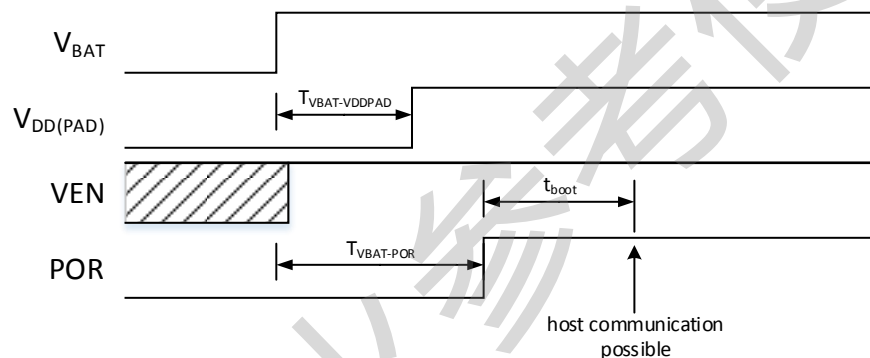


Figure 21.VEN tie high at board level

8.7.1.2 VEN controlled by host controller

SL6550 start booting after VEN is set high, and t_{boot} is required before host communication possible.

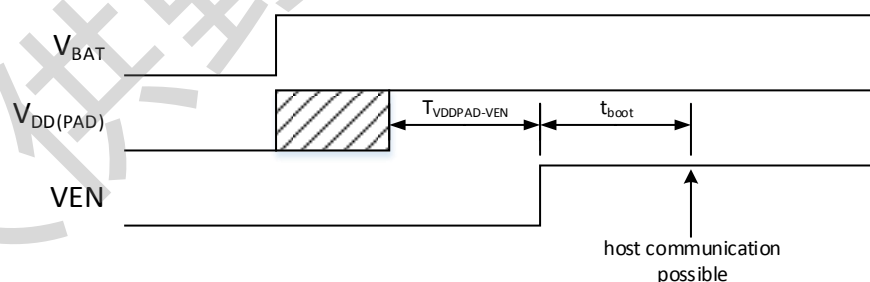


Figure 22.VEN controlled by host controller

8.7.1.3 VEN is set high before $V_{DD(PAD)}$ available

In some application, power pin V_{BAT} directly connected to the battery and $V_{DD(PAD)}$ is generated from a PMU. When battery voltage is too low, PMU may not be able to generate $V_{DD(PAD)}$ required. When device been recharged, $V_{DD(PAD)}$ is available again.

Since SL6550 pins are biased from $V_{DD(PAD)}$, disappearance of $V_{DD(PAD)}$ may cause pins been incorrectly biased. All pins except VEN are automatically disabled when $V_{DD(PAD)}$ is not available to avoid information lost. VEN issue is handled by setting internal register VEN_reg

to 1(if host can predict the disappearance of $V_{DD(PAD)}$) or reboot SL6550 by tie low VEN and then tie high it after $V_{DD(PAD)}$ available again.

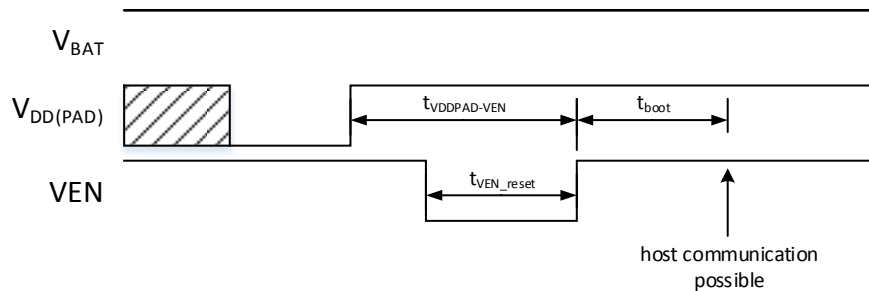


Figure 23.Reset by VEN after $V_{DD(PAD)}$ been cut-off

8.7.1.4 $V_{DD(SIM_PMU_X)}$ power up sequence

$V_{DD(SIM_X)}$ is powered by either $V_{DD(SIM_PMU_X)}$ or internal regulator. $V_{DD(SIM_PMU_X)}$ is from board level PMU or anything else. When $V_{DD(SIM_PMU_X)}$ is powered on, V_{BAT} and $V_{DD(PAD)}$ shall be already available. Internal regulator enable is controlled by register which can be configured via host interface.

It's suggested that when doing switching between two power sources, make sure that disable the power supply in use first, and enable the power supply to be used second.

8.7.1.5 Power down sequence

When $V_{DD(PAD)}$ is not available, all digital interfaces are disabled except VEN. To avoid unexpected behavior of SL6550, it's required to drive VEN low before $V_{DD(PAD)}$ been powered off during power down sequence.

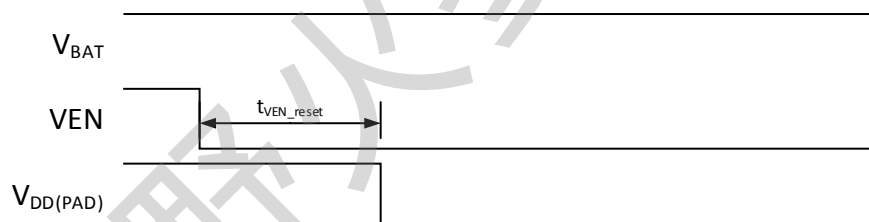


Figure 24.SL6550 power down sequence

When $V_{DD(SIM_X)}$ is powered by $V_{DD(SIM_PMU_X)}$, powering off $V_{DD(SIM_PMU_X)}$ may cause unexpected behavior on SWP interface. So when $V_{DD(SIM_PMU_X)}$ is selected as the power supply of $V_{DD(SIM_X)}$, it's required to drive VEN low before $V_{DD(SIM_PMU_X)}$ been powered off during power down sequence.

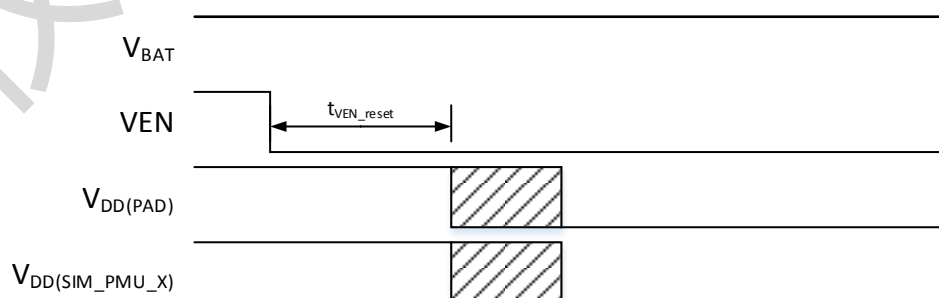


Figure 25.SL6550 power down sequence when using $V_{DD(SIM_PMU_X)}$

8.7.1.6 Firmware download

SL6550 allows its firmware been upgrade via host interface. To enter download mode, drive DWL_REQ high and do reset of SL6550. If doing reset via host interface command, it's required that fastboot option is disabled.

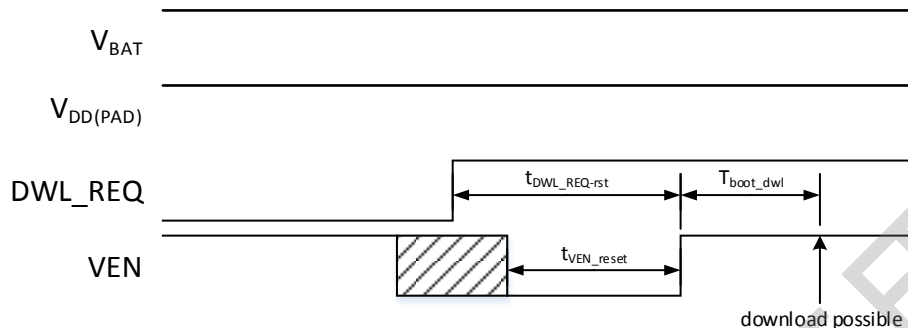


Figure 26.SL6550 enter download mode with VEN reset

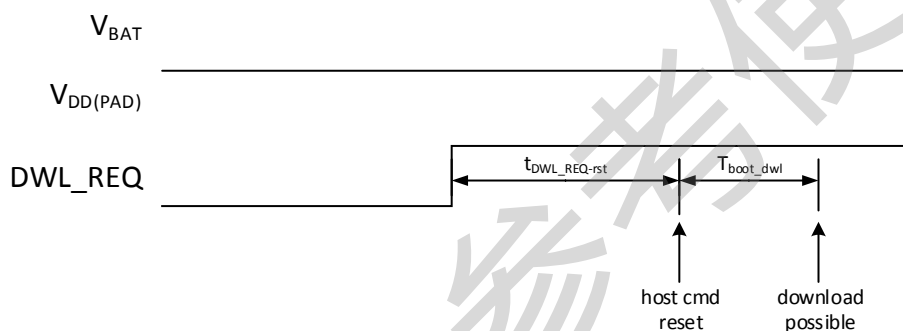


Figure 27.SL6550 enter download mode with host command reset

8.8 Contactless Interface

SL6550 could support various communication modes at different transfer speed and modulation schemes. The following chapters will describe more detail communication mode.

8.8.1 Reader/Writer communication modes

- PCD for ISO/IEC 14443A/MIFARE(NFC forum Types 2 Tag and Type 4A Tag)
- PCD for ISO/IEC 14443B(NFC forum Type 4BTag)
- PCD for NFC forum Type 1 Tag
- PCD for NFC forum Type 3 Tag
- VCD for NFC forum Type 5 Tag

8.8.1.1 PCD for ISO/IEC 14443A

The PCD mode for NFC forum Type 1 Tag, Type 2 Tag and Type4 Tag type A is the general PCD to PICC communication scheme according to the ISO/ICE 14443A specification.

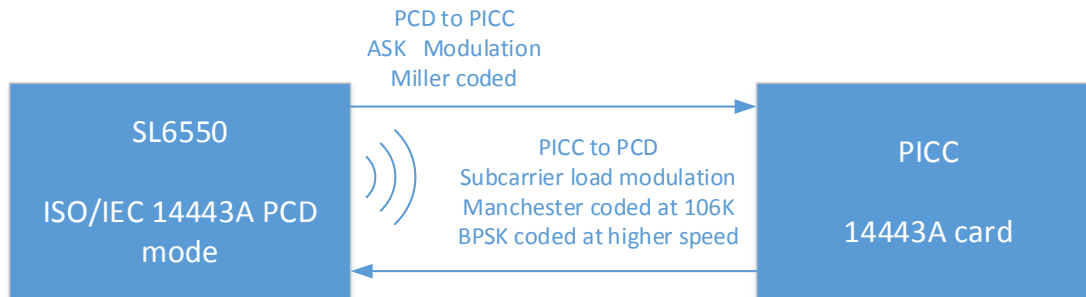


Figure 28. PCD for ISO/IEC 14443A communication

Table 14. Communication overview for ISO/IEC 14443A PCD mode

direction		ISO/IEC 14443A / Mifare	ISO/IEC 14443A		
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
SL6550->PICC Transmit	coding	Miller	Miller	Miller	Miller
	modulation on SL6550	ASK 100%	ASK 100%	ASK 100%	ASK 100%
PICC->SL6550 Receive	coding	Manchester	BPSK	BPSK	BPSK
	subcarrier	fc/16	fc/16	fc/16	fc/16
	modulation on PICC	subcarrier load	subcarrier load	subcarrier load	subcarrier load

fc : 13.56MHz

8.8.1.2 PCD for ISO/IEC 14443B

The PCD mode for NFC forum Type4 Tag type B is the general PCD to PICC communication scheme according to the ISO/ICE 14443B specification.

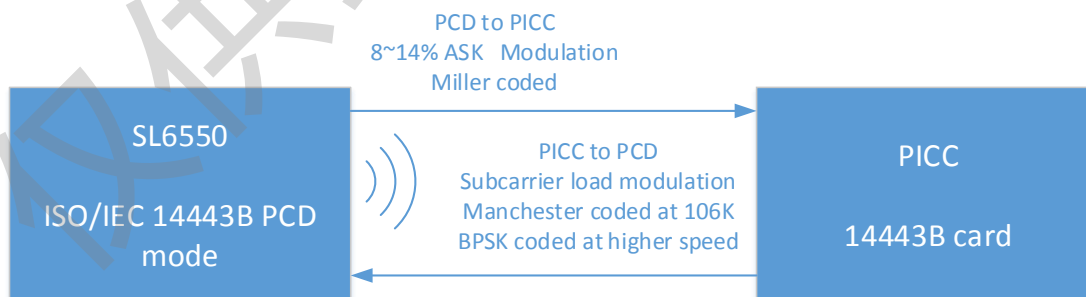


Figure 29. PCD for ISO/IEC 14443B communication

Table 15. Communication overview for ISO/IEC 14443B PCD mode

direction		ISO/IEC 14443B			
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
SL6550->PICC	coding	NRZL	NRZL	NRZL	NRZL

Transmit	modulation on SL6550	ASK8~14%	ASK8~14%	ASK8~14%	ASK8~14%
PICC->SL6550 Receive	coding	BPSK	BPSK	BPSK	BPSK
	subcarrier	fc/16	fc/16	fc/16	fc/16
	modulation on PICC	subcarrier load	subcarrier load	subcarrier load	subcarrier load

fc : 13.56MHz

8.8.1.3 PCD for NFC forum Type 3 Tag, Felica mode

The PCD mode for NFC forum Type 3 Tag, Felica mode is the general PCD to PICC communication scheme according to the Felica specification.

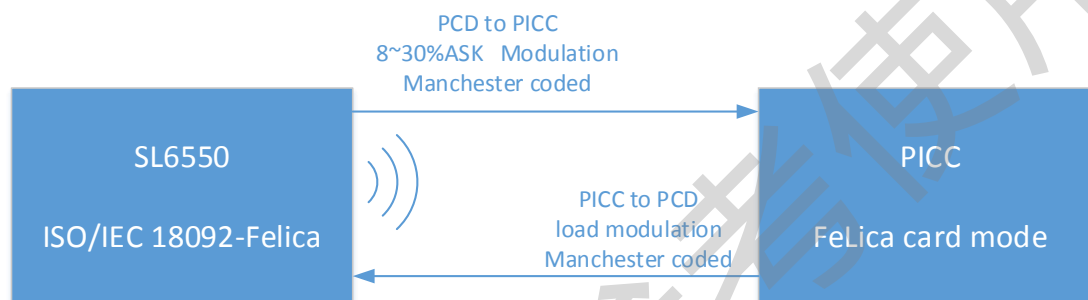


Figure 30. PCD for NFC forum Type 3 Tag, Felica communication

Table 16. Communication overview for NFC forum Type 3 Tag, Felica PCD mode

direction		felica212K	felica424K
	Transfer speed	212 kbit/s	424 kbit/s
SL6550->PICC Transmit	coding	Manchester	Manchester
	modulation on SL6550	ASK 8%~12%	ASK 8%~12%
PICC->SL6550 Receive	coding	Manchester	Manchester
	modulation on PICC	load	load

fc : 13.56MHz

8.8.1.4 VCD for NFC forum Type 5 Tag

The VCD mode for NFC forum Type 5 Tag is the general VCD to VICC communication scheme according to the ISO/IEC 15693 specification. SL6550 supports VICC using both 26.48 kbit/s and 6.62kbit/s with single subcarrier.

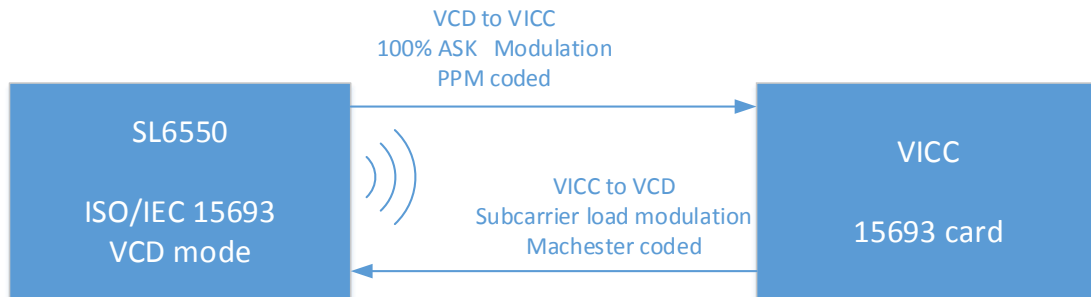


Figure 31. VCD for NFC forum Type 5 Tag communication

Table 17. Communication overview for NFC forum Type 3 Tag, Felica PCD mode

direction	Transfer speed	1.65 kbit/s	26.48 kbit/s
SL6550->VICC Transmit	coding	PPM 1/4	PPM 1/256
	modulation on SL6550	ASK 10%/100%	ASK 10%/100%
PICC->SL6550 Receive	Transfer speed	6.62 kbit/s	26.48 kbit/s
	coding	Manchester	Manchester
	subcarrier	fc/32	fc/32
	modulation on VICC	subcarrier load	subcarrier load

fc : 13.56MHz

8.8.2 Card mode

SL6550 can be configured as various card mode, they are

- PICC for ISO/IEC 14443A
- PICC for ISO/IEC 14443B
- NFC forum Type 3 Tag
- NFC forum Type 4A/B Tag

8.8.2.1 PICC for ISO/IEC 14443A, Type 4A Tag

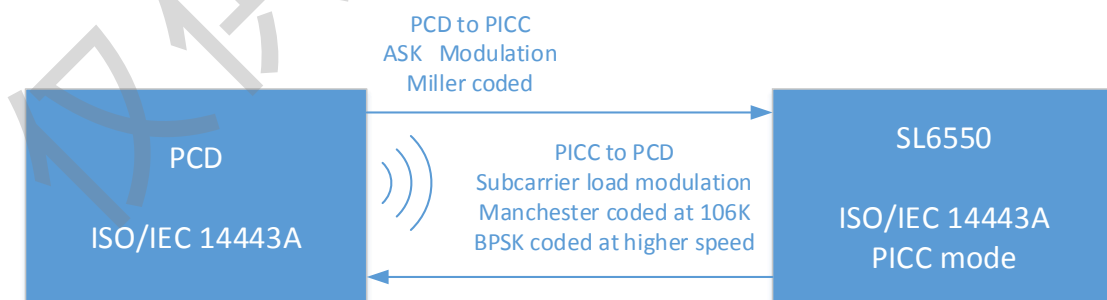


Figure 32. PICC for ISO/IEC 14443A, Type 4A Tag communication

Table 18. communication overview for ISO/IEC 14443A PICC mode, Type 4A Tag

direction		ISO/IEC 14443A	ISO/IEC 14443A
-----------	--	----------------	----------------

NFC Controller

	Transfer speed	106kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
PCD->SL6550 Receive	coding	Miller	Miller	Miller	Miller
	modulation on PCD	ASK 100%	ASK >25%	ASK >25%	ASK >25%
SL6550->PCD Transmit	coding	Manchester	BPSK	BPSK	BPSK
	subcarrier	fc/16	fc/16	fc/16	fc/16
	modulation on SL6550	subcarrier load	subcarrier load	subcarrier load	subcarrier load

fc : 13.56MHz

8.8.2.2 PICC for ISO/IEC 14443B, Type 4B Tag

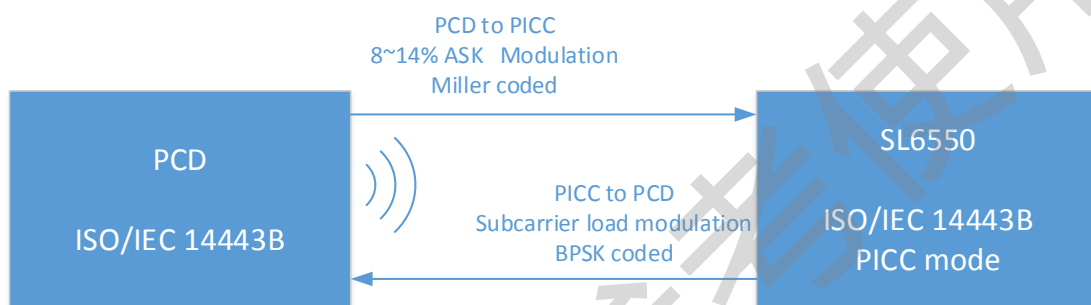


Figure 33. PICC for ISO/IEC 14443B, Type 4B Tag communication

Table 19. communication overview for ISO/IEC 14443B PICC mode, Type 4B Tag

		ISO/IEC 14443B			
	Transfer speed	106 kbit/s	212 kbit/s	424 kbit/s	848 kbit/s
PCD->SL6550 Receive	coding	NRZL	NRZL	NRZL	NRZL
	modulation on PCD	ASK8~14%	ASK8~14%	ASK8~14%	ASK8~14%
SL6550->PICC Transmit	coding	BPSK	BPSK	BPSK	BPSK
	subcarrier	fc/16	fc/16	fc/16	fc/16
	modulation on SL6550	subcarrier load	subcarrier load	subcarrier load	subcarrier load

fc : 13.56MHz

8.8.2.3 NFC forum Type 3 Tag

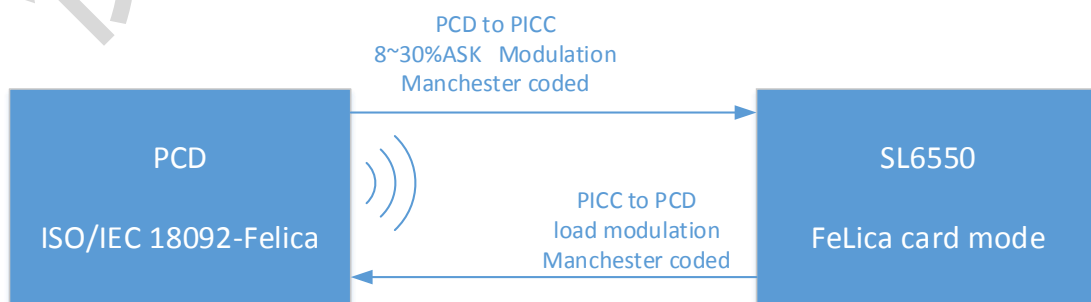


Figure 34. NFC forum Type 3 Tag communication

Table 20. communication overview for NFC forum Type 3 Tag

direction		felica212K	felica 424K
	Transfer speed	212 kbit/s	424 kbit/s
PCD->SL6550 Receive	coding	Manchester	Manchester
	modulation on PCD	ASK 8%~30%	ASK 8%~30%
SL6550->PCD Transmit	coding	Manchester	Manchester
	modulation on SL6550	load	load

8.8.3 ISO/IEC 18092, NFCIP-1 communication modes

SL6550 supports the Active Initiator, Active Target, Passive Initiator and Passive Target communication modes at the transfer speeds 106kbits/s, 212kbits/s and 424 kbits/s as defined in the NFCIP-1 standard.

- NFC Initiator: generates RF field at 13.56M and starts the NFCIP-1 communication.
- NFC Target: response to NFC Initiator command either in a load modulation scheme in Passive communication mode or using a self generated and self modulated RF field for Active communication mode

The NFCIP-1 communication differentiates between Active and Passive communication modes.

Active communication mode means both the NFC Initiator and NFC Target are using their won RF field to transmit data

Passive communication mode means that the NFC Target answers to an NFC Initiator command in a load modulation scheme. The NFC Initiator is active in term of generating the RF field.

8.8.3.1 Active communication mode

Active communication mode means both the NFC Initiator and the NFC Target are using their own RF field to transmit data.

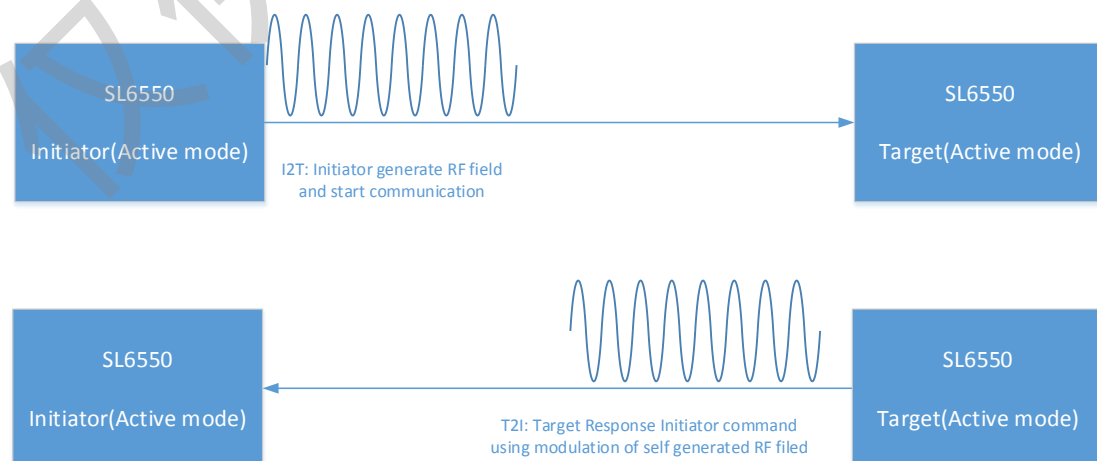


Figure 35. Active communication mode

Table 21. Overview for Active communication mode

direction	ISO/IEC 18092, NFCIP-1			
	Transfer speed	106kbit/s	212 kbit/s	424 kbit/s
Initiator->Target	coding	Miller	Manchester	Manchester
	modulation on SL6550	ASK 100%	ASK 8%~30%	ASK 8%~30%
Target->Initiator	coding	Miller	Manchester	Manchester
	modulation on SL6550	ASK 100%	ASK 8%~30%	ASK 8%~30%

8.8.3.2 Passive communication mode

Passive communication mode means that when the Initiator is generating the RF field and the Target responds to an Initiator command in a load modulation scheme.

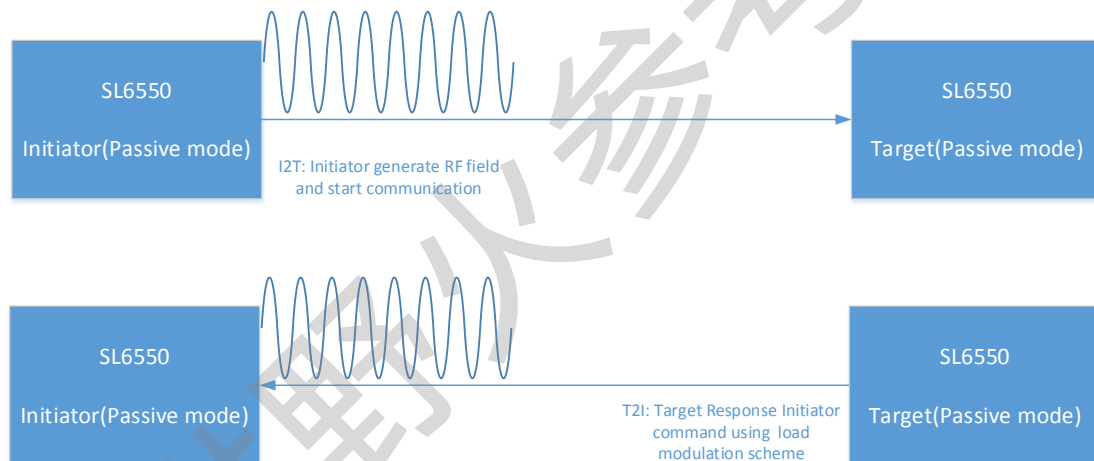


Figure 36. Passive communication mode

Table 22. Overview for Passive communication mode

		ISO/IEC 18092, NFCIP-1		
	Transfer speed	106kbit/s	212 kbit/s	424 kbit/s
PCD->PICC	coding	Miller	Man	Man
	modulation on SL6550	ASK 100%	ASK 8%~30%	ASK 8%~30%
PICC->PCD Passive	coding	Man	Manchester	Manchester
	subcarrier	fc/16	No	No
	modulation on SL6550	subcarrier	load	load

fc : 13.56MHz

9. Limiting values

Table 23. Limiting values

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD(PAD)}	V _{DD(PAD)} supply voltage	supply voltage for host interface	-	2.35	V
V _{DD(GPIO)}	V _{DD(GPIO)} supply voltage	supply voltage for host interface	-	2.35	V
V _{DD(UP)}	V _{DD(UP)} input supply voltage	supply voltage for host interface	-	7	V
V _{BAT}	battery supply voltage		-	6	V
V _{DD(SIM_PMU_X)}	UICC input power from external PMU	[1]	-	4	V
V _{SIM_IO_PULLDOWN_X}	voltage on pins SIM_IO_PULLDOWN_X	[1]	-	4	V
V _{ESD}	electrostatic discharge voltage	HBM; 1500Ω, 100 pF;	-	1.5	KV
		CDM; field induced model;	-	500	V
T _{stg}	storage temperature		-40	+85	°C
P _{tot}	total power dissipation	all modes[2]	-	620	mW
V _{RXN(i)}	RXN input voltage		0	2.5	V
V _{RXNP(i)}	RXP input voltage		0	2.5	V

[1]. With X = 1 or 2.

[2]. The design of the solution shall be done so that for the different use cases targeted the power to be dissipated from the field or generated by SL6550 does not exceed this value.

10. Recommended operating condition

Table 24. Operating condition

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T _{amb}	ambient temperature	JEDEC PCB-0.5	-25	-	+85	°C
V _{BAT}	battery supply voltage	Card Emulation and Passive Target; V _{DD(UP)} > 2.9 V; V _{SS} = 0V	2.5	-	5.5	V
		Reader, Active Initiator and Active Target; V _{DD(UP)} > 3.1 V; V _{SS} = 0V	2.8	-	5.5	V
V _{DD(UP)}	V _{DD(UP)} input supply voltage	Card Emulation and Passive Target; V _{SS} = 0V	2.8	-	5.8	V
		Reader, Active Initiator and	3.1	-	5.8	V

Table 24. Operating condition

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Active Target; $V_{SS} = 0V$				
$V_{DD}(SIM_PMU_X)$	UICC input power from external PMU	class C, UICC compliant to ETSI 102 221 rel 9	1.65	-	1.98	V
		class C, UICC compliant to ETSI 102 221 rel 12; $I_{VDD}(SIM_PMU_X) = 60mA$	1.75	-	1.85	V
		class B; $I_{VDD}(SIM_PMU_X) = 50mA$	2.91	-	3.3	V
$V_{DD}(PAD)$	$V_{DD}(PAD)$ supply voltage	supply voltage for host interface; $V_{SS} = 0V$	1.65	1.8	1.95	V
$V_{DD}(GPIO)$	$V_{DD}(GPIO)$ supply voltage	supply voltage for GPIO; $V_{SS} = 0V$	1.65	1.8	1.95	V
$V_{DD}(SIM_X)$	UICC power supply	no $V_{DD}(SIM_PMU_X)$; $I_{VDD}(SIM_X) = 10m$	1.625	-	1.98	V
P_{tot}	total power dissipation	PCD mode at typical $V_{DD}(TX) = 5.25V$, $V_{DD}(UP) = 5.8V$ and $V_{BAT} = 3.6V$; includes power from V_{BAT} and $V_{DD}(UP)$	-	-	620	mW
		in Hard Power Down state; $V_{BAT} = 3.6V$; $T = 25^\circ C$	-	10.5	16	μA
		in Standby state; $V_{BAT} = 3.6V$	-	-	-	-
		enhanced RF detector	-	32	52	μA
		low sensitivity RF detector	-	21	36	μA
		in low-power polling loop; $V_{BAT} = 3.6V$; $T = 25^\circ C$; loop time = 500 ms	-	100	-	μA
I_{BAT}	battery supply current	continuous total current consumption in PCD mode at $V_{BAT} = 3.6V$ [4]	-	-	290	mA
$I_{th}(lim)$	current limit threshold	current limiter on transmitter [4]	270	300	330	mA

[1]. V_{SS} represents $V_{SS}(PAD)$ and $V_{SS}(TX)$.

[2]. $X = 1$ or 2 .

[3]. External clock on NFC_CLK_XTAL1 must be LOW.

[4]. This is considering an antenna tuned to sink maximum 250mA continuous current from the transmitter. The antenna shall be tuned to never exceed this 250mA maximum current.

11. Thermal characteristics

Table 25. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air with exposed pad soldered on a 2 layer JEDEC PCB	-	52	-	K/W

12. Characteristics

仅供野火参考使用

13. Package outline

VFBGA64: plastic very thin fine-pitch ball grid array package; 64 balls

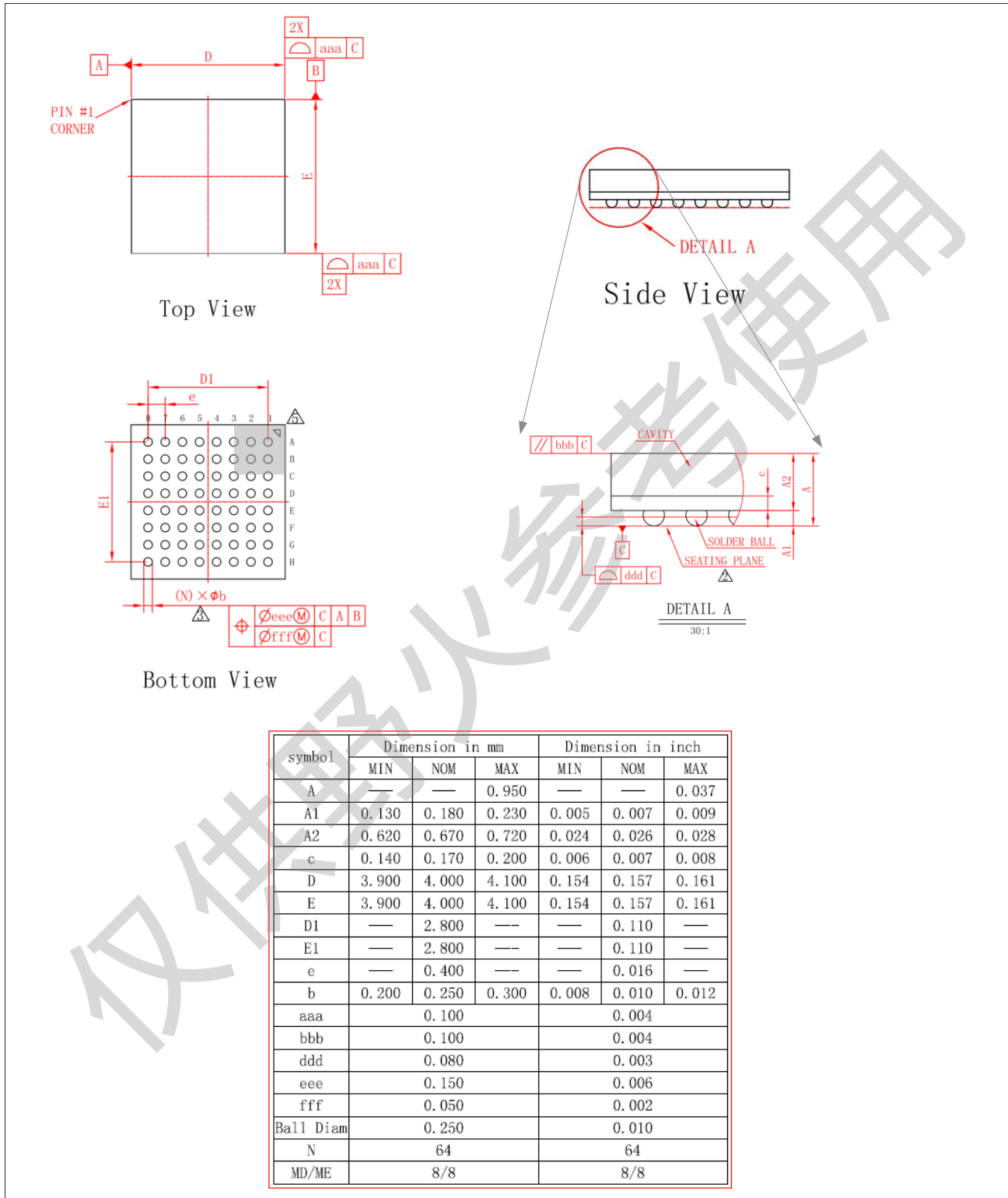


Figure 37. Package outline

14. Package marking

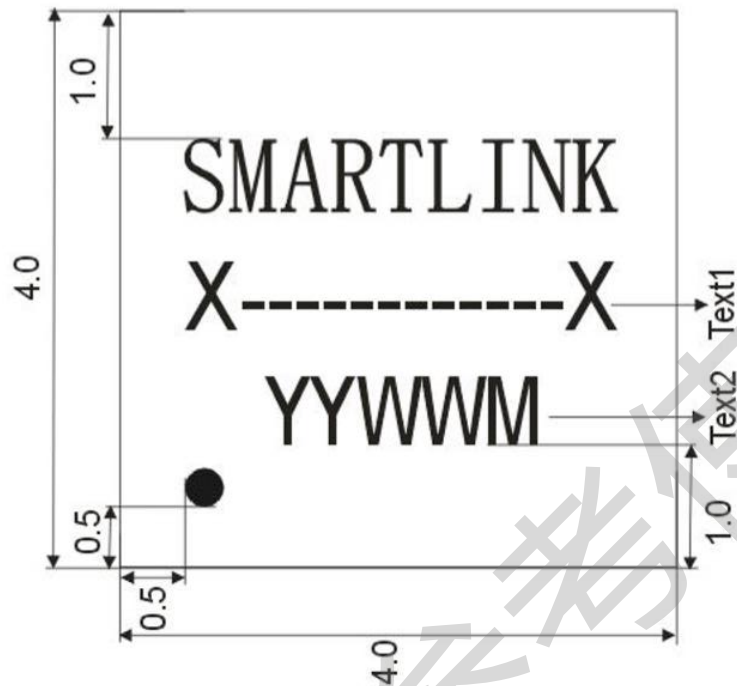


Figure 38. SL6550 package marking (top view)

Table 26. Package marking code

Package marking code		Max Chars	Description
Line 1	SMARTLINK	/	Company logo
Line 2	X-----X	8	product model
Line 3	YYWWM	5	manufacturing code including: • manufacturing year and week, 2 digits: ✓ YY: year, system generated ✓ WW: week, system generated • manufacturing fixed code, 1 digits: ✓ M: the production version number

15. Soldering of SMD packages

16. Abbreviations

Table 27. Abbreviations

Acronym	Description
ASK	Amplitude Shift keying
ASK modulation index	The ASK modulation index is defined as the voltage ratio $(V_{max} - V_{min}) / (V_{max} + V_{min}) * 100\%$
Automatic device discovery	Detect and recognize any NFC peer devices (NFC Initiator or NFC Target) like: NFC Initiator or NFC Target, ISO/IEC 14443-3, -4 Type A&B PICC, MIFARE Standard and Ultralight PICC, ISO/IEC 15693 VICC
BPSK	Bit Phase Shift Keying
Card Emulation	The IC is capable of handling a PICC emulation on the RF interface including part of the protocol management. The application handling is done by the host controller
LDO	Low Drop Out
NFC	Near Field Communication
P2P	Peer to Peer
PCD	Proximity Coupling Device. Definition for a Card reader/writer device according to the ISO/IEC 14443 specification or MIFARE
PICC	Proximity Interface Coupling Card. Definition for a contactless Smart Card according to the ISO/IEC 14443 specification
PCD -> PICC	Communication flow between a PCD and a PICC according to the ISO/IEC 14443 specification or MIFARE
PICC-> PCD	Communication flow between a PICC and a PCD according to the ISO/IEC 14443 specification or MIFARE
PMOS	P-channel MOSFET
PMU	Power Management Unit
SPI-bus	Serial Peripheral Interface bus
VCO	Voltage Controlled Oscillator

17. References

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- [12]. EMVCo — EMV Contactless Specifications for Payment Systems - Book D - EMV Contactless Communication Protocol Specification”, version 2.3.1, December 2013.

18. Legal information

19. Contact information

Any product demand, please contact us!

Table 28. Connect Information

Company Website	http://www.smartlinkmicro.com
Company Address	A-Tower, East Bldg. 14, Courtyard #10, Xibeiwang East Road, Haidian Dist., Beijing, China.
P.C.	100193
Tel.	+86-10-56345288 Ext.9
Fax.	+86-10-56345288
Technical Support	Please email to: support@smartlinkmicro.com
Business Cooperation	Please email to: marketing@smartlinkmicro.com

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